STM32F407GDIE
Die description

STM32F407xx die and wafer delivery description

Product information

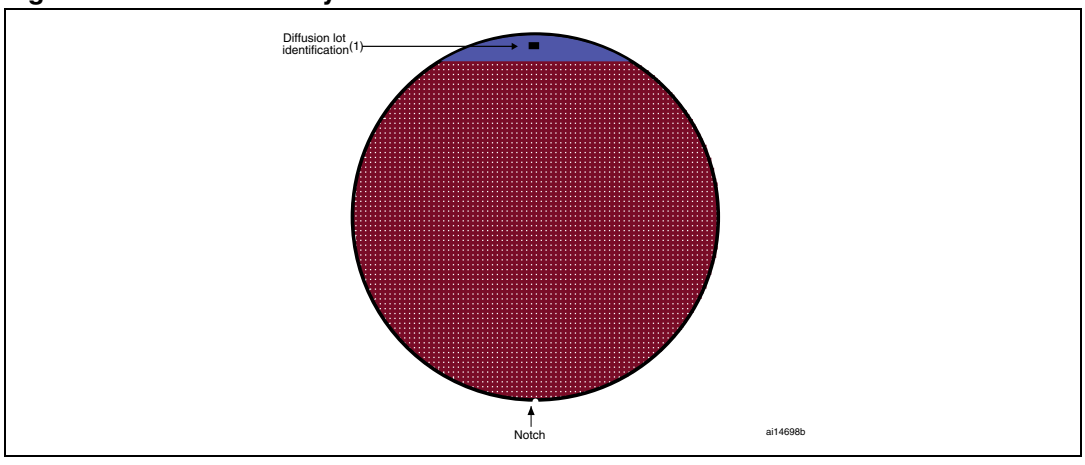
Table 1. Bare die codification

Die part number	Order code	Temperature range	Equivalent packaged parts	Flash program memory (KB)	SRAM (KB)	Number of pins /pads
STM32F407GDIE	STM32F407GDIE1	–40 to 85 °C	STM32F407IGT6 STM32F407IGH6	1024	192	64, 100, 144, 176+25, 90

Wafer and die features

- Wafer size: 8 inches
- Die identification: R413
- Die size (X,Y): 3924 x 4178 µm
- Die stepping (X,Y): 4004 x 4258 µm
- Die thickness: 375 ± 25 µm
- Scribe street (X,Y): 80 x 80 µm
- Die finish front side: HDP USG/SiN
- Die finish back side: Raw silicon
- ESD sensitivity class Class II [500,1999]
- Wafer type (Si, GaAs, Others): Si
- Process type: CMOS
- Pad number per die: 199
- Laser trimming: not applicable

Figure 1. Wafer delivery form: 8-inch unsawn wafer



1. For the Diffusion lot identification, refer to *Diffusion lot identification*

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1 Description

The STM32F40x family is based on the high-performance ARM® Cortex™-M4 32-bit RISC core operating at a frequency of up to 168 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security. The Cortex-M4 core with FPU will be referred to as Cortex-M4F throughout this document. The STM32F40x family incorporates high-speed embedded memories (Flash memory up to 1 Mbyte, up to 192 Kbytes of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The devices also feature an adaptive real-time memory accelerator (ART Accelerator™) which allows to achieve a performance equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 168 MHz. This performance has been validated using the CoreMark benchmark.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers. a true random number generator (RNG). They also feature standard and advanced communication interfaces. New advanced peripherals include an SDIO, an enhanced flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more), and a camera interface for CMOS interface.

For electrical and functional information, please refer to the datasheet and reference manual of the equivalent packaged part. The electrical characteristics are the same, with a restricted temperature range, except for a few parameters.

The values that change are specified in *Table 2* below. For other characteristics, please refer to the high-density STM32F407xx datasheet available from the STMicroelectronics website: www.st.com.

Table 2. HSI oscillator accuracy(1) (2)

Symbol	Parameter	Conditions	Min	Max	Unit
ACC_{HSI}	Factory calibrated accuracy of the HSI oscillator	T_A = –40 to 85 °C	–8.0	4.5	%
		T_A = 25 °C	–1.0	1.0	

1. Guaranteed by design, not tested in production.
2. V_{DD} = 3.3 V.

2 Die description

2.1 Bond pad description

Refer to *Section 7* for specific handling terms and conditions.

Table 3. Wire bond pad metal

Wire bond pad metal	Composition	Thickness (µm)
Metal 1	TaN/Ta/CuSeed/Cu	0.280
Metal 2	TaN/Ta/CuSeed/Cu	0.360
Metal 3	TaN/Ta/CuSeed/Cu	0.360
Metal 4	TaN/Ta/CuSeed/Cu	0.360
Metal 5	TaN/Ta/CuSeed/Cu	0.360
Metal 6	TaN/Ta/CuSeed/Cu	0.820
Metal 7	Ti/AlCu/TiN	1.200

I/O type: CUP (circuit under pad).

Figure 2. Pad diagram

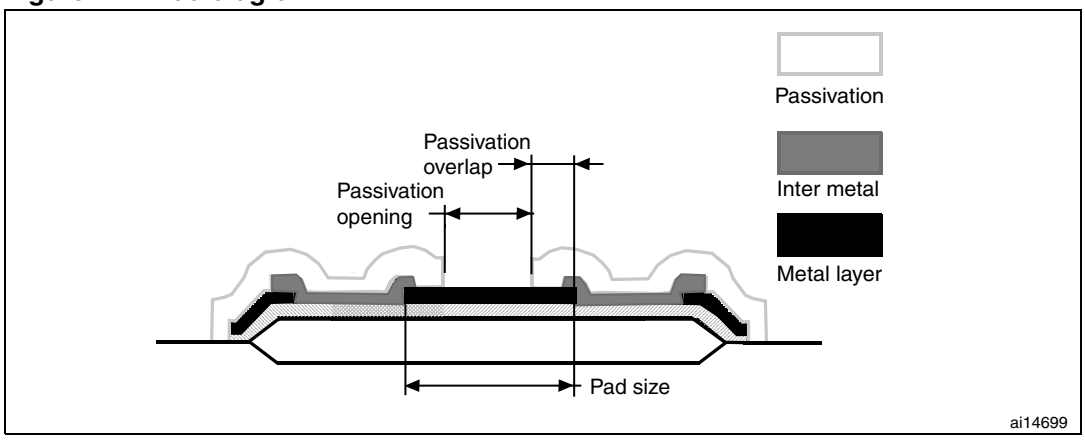


Table 4. Bond pads

Number of pads	Pad size	Passivation opening size	Minimum passivation and pad overlap (µm)
199	X = 65 µm, Y = 134 µm	X = 59 µm, Y = 123 µm	2

Table 5. Assembly features (critical dimensions)

Wire quantity	Wire material type	Wire diameter	Bond pad windows (X,Y)	Minimum pitch	Wire bond pad placement
N/A	Gold	20 µm	59 µm x 59 µm	65 µm	100%

2.2 Wafer processing and assembly

2.2.1 Good dice

The bad dice are identified by inkless pass/fail wafer e-map. The inkless e-map file is provided in STIF format. Refer to package information PI0301 “*Inkless 8” wafers”,* for a description of the inkless e-map that allows to transfer wafer information between ST on the one hand, and subcontractors and customers, on the other hand.

Number of dice per wafer	Gross dice:	1640

2.2.2 Back-lapping

Back-lapping is permitted on these wafers to reduce wafer thickness. ST does not perform additional back-lapping in house for these products, it has to be done by a sub-contractor.

Minimum thickness allowed:	75 µm

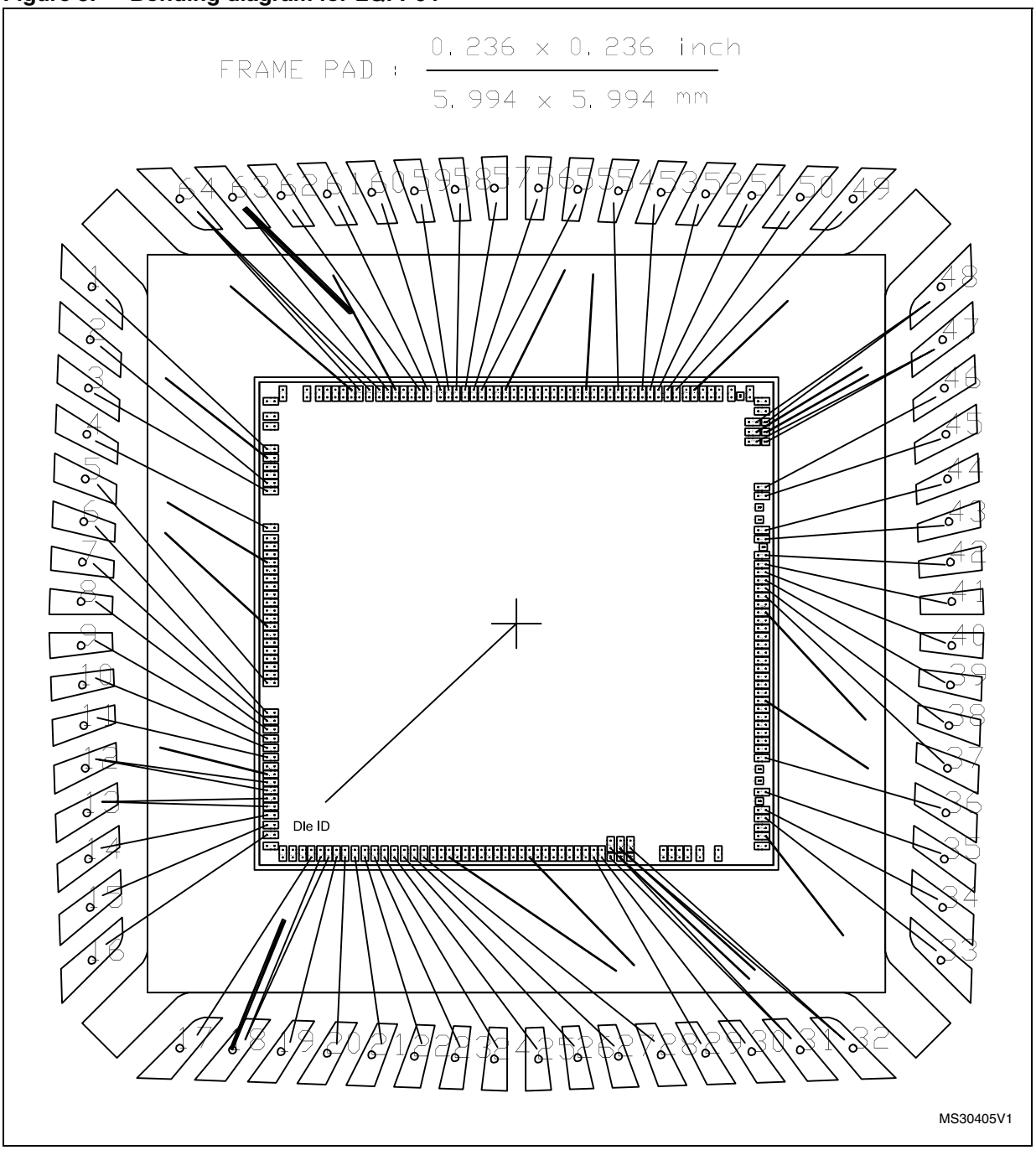
2.2.3 Assembly

The Autocad or GDS files of pad opening are available upon request.

3 Bonding diagrams and pinout/ballout schematics

3.1 LQFP64 - 64-pin low-profile quad flat package

Figure 3. Bonding diagram for LQFP64



3.2 LQFP100 - 100-pin low-profile quad flat package

Figure 4. Bonding diagram for LQFP100

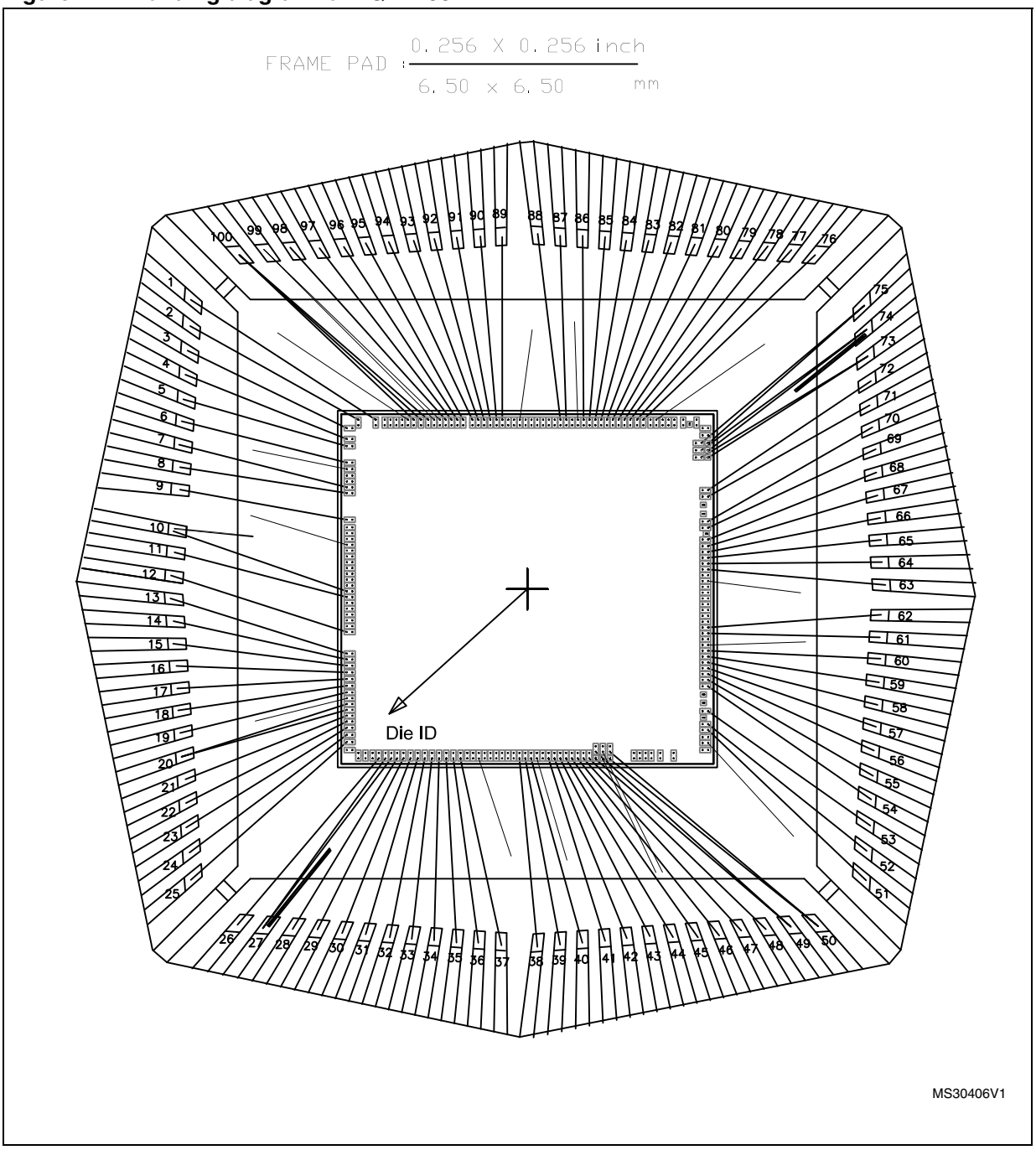
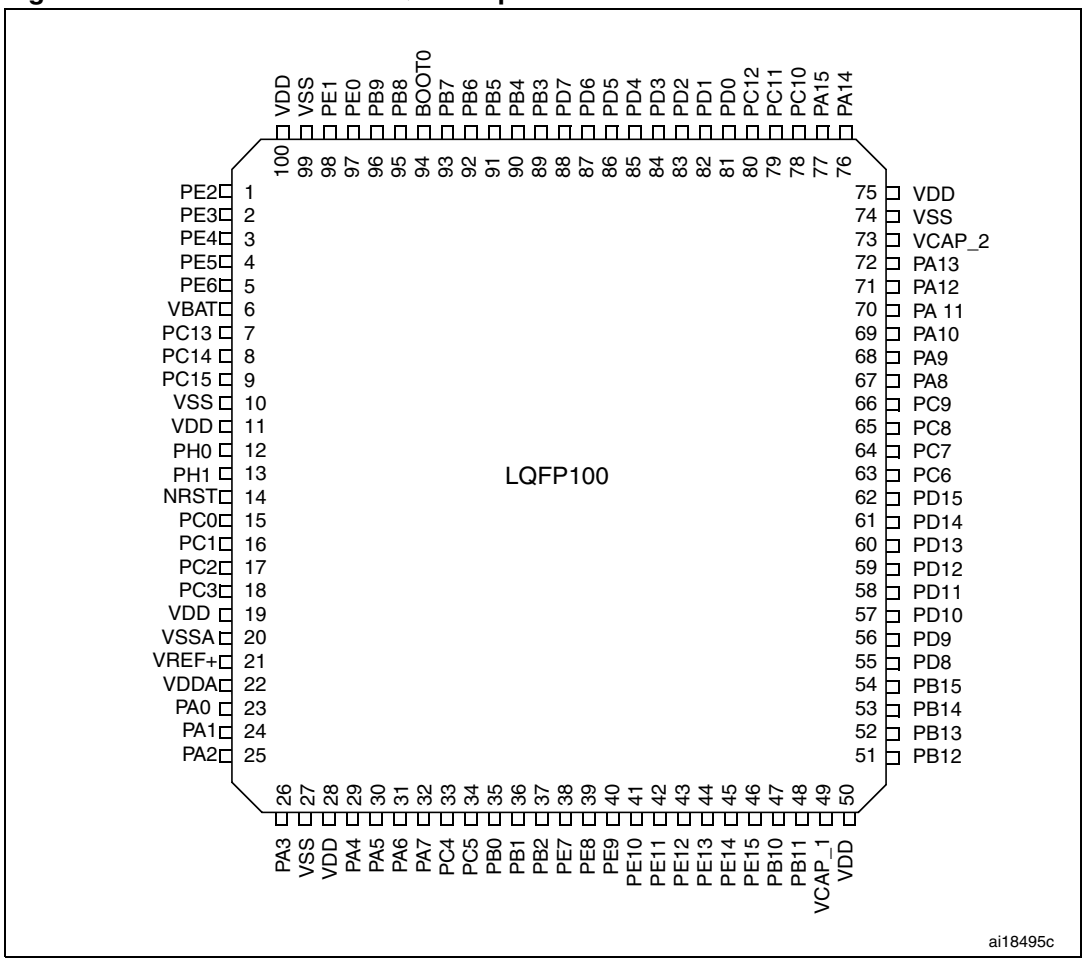


Figure 5. STM32F407GDIE LQFP100 pinout



3.3 LQFP144 - 144-pin low-profile quad flat package

Figure 6. Bonding diagram for LQFP144

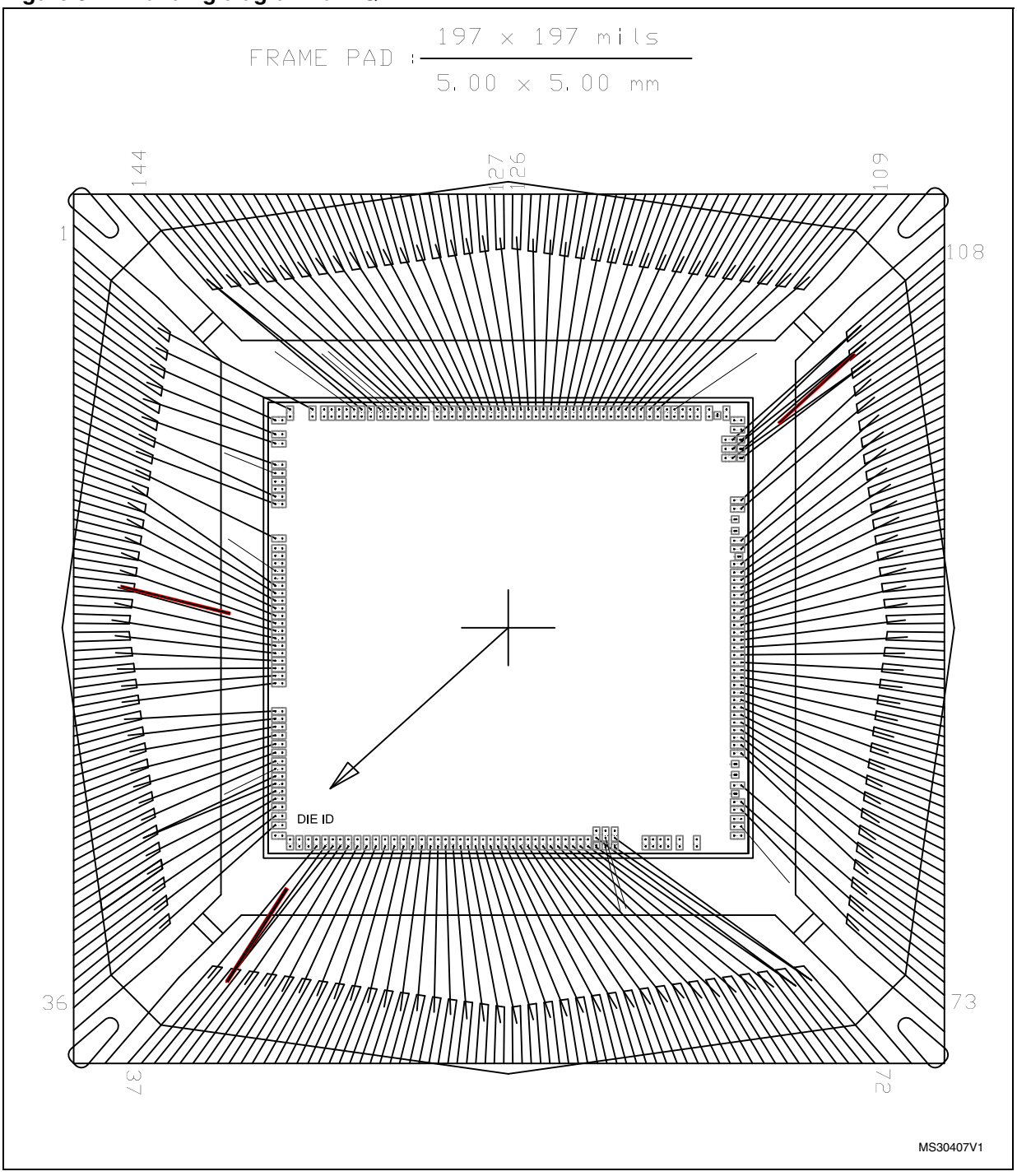
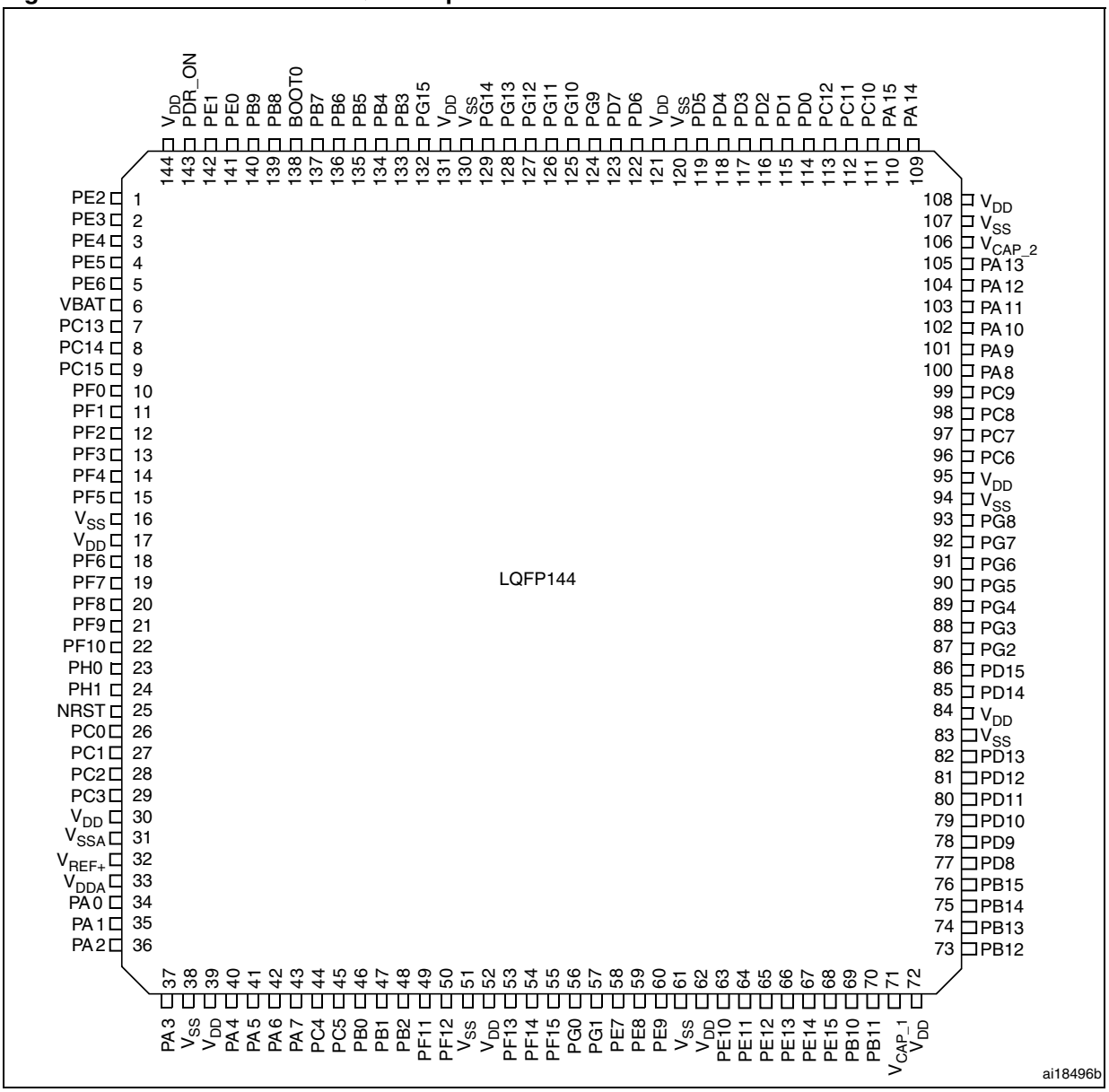


Figure 7. STM32F407GDIE LQFP144 pinout



3.4 LQFP176- 176-pin low-profile quad flat package

Figure 8. Bonding diagram for LQFP176

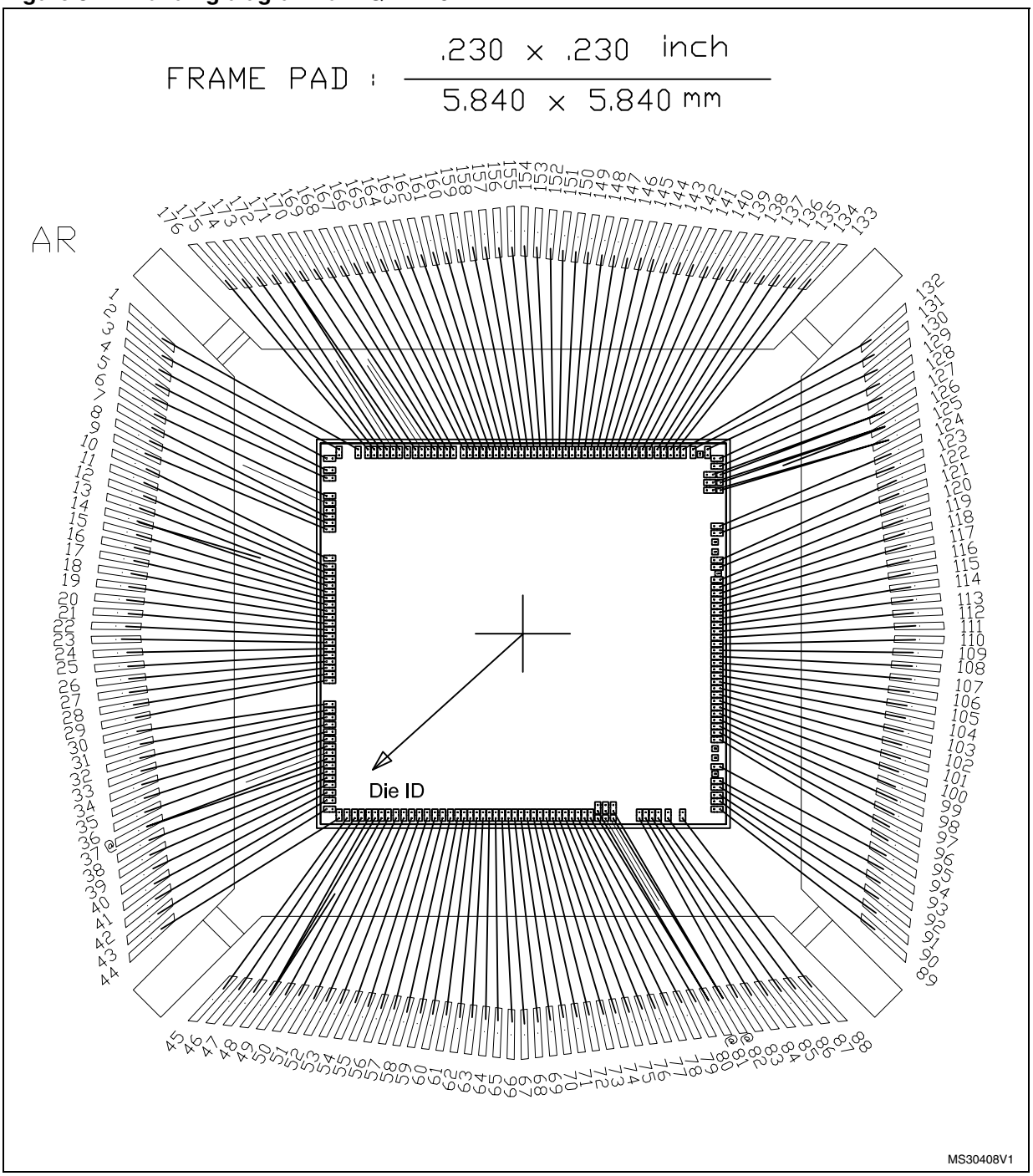
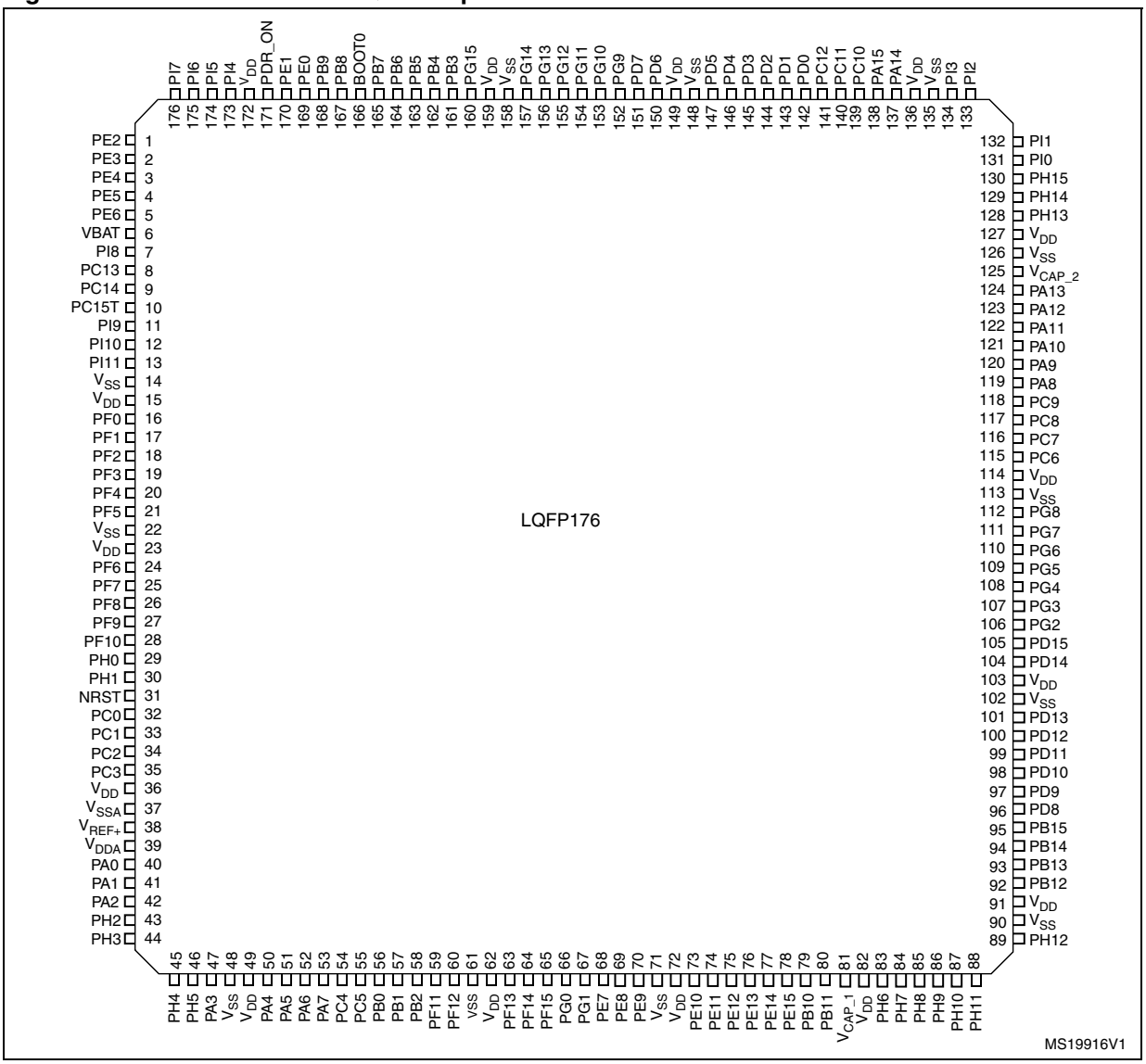


Figure 9. STM32F407GDIE LQFP176 pinout



3.5 UFBGA176+25 - ultra thin fine pitch ball grid array package

Figure 10. Bonding diagram for UFBGA176+25

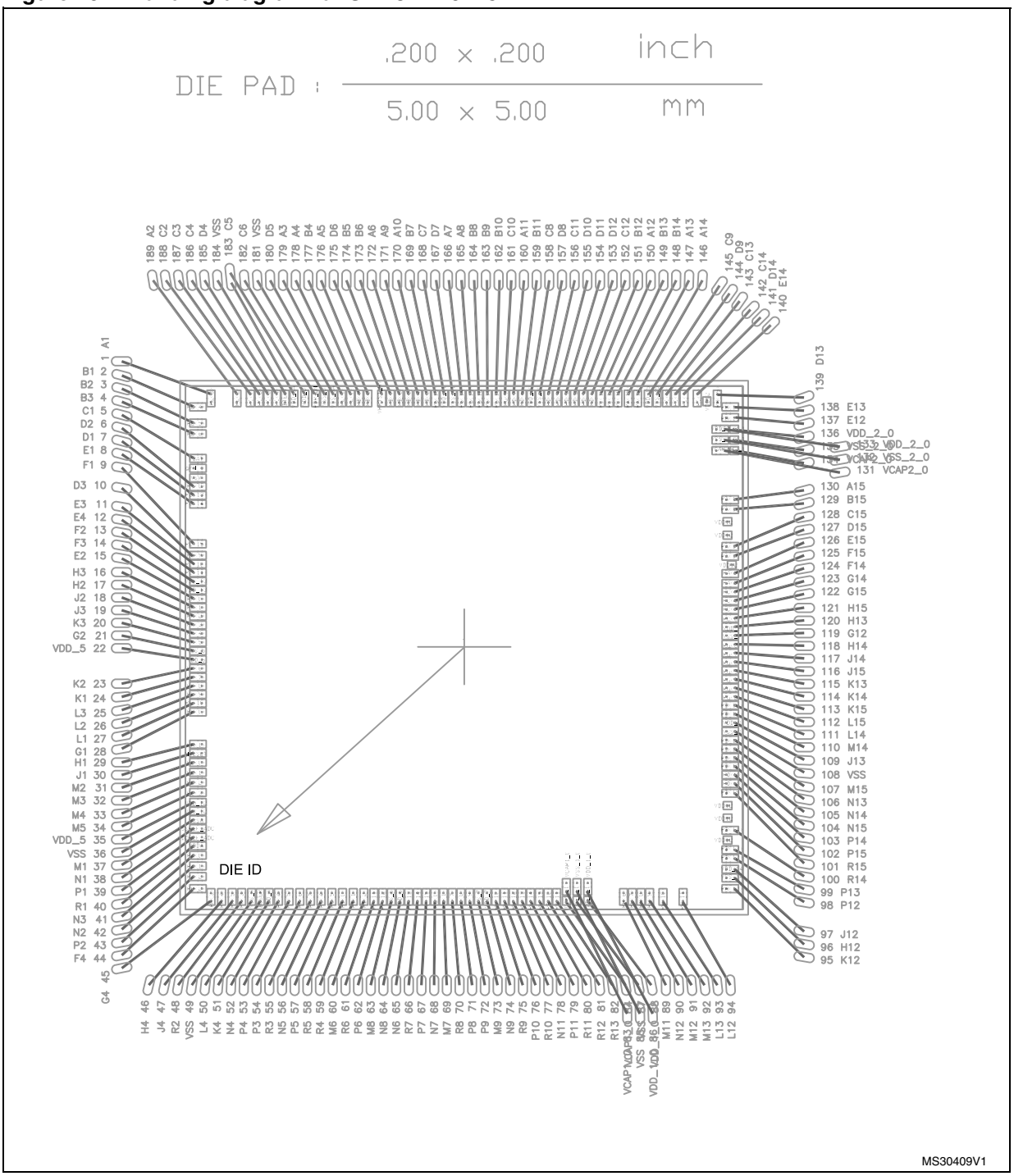
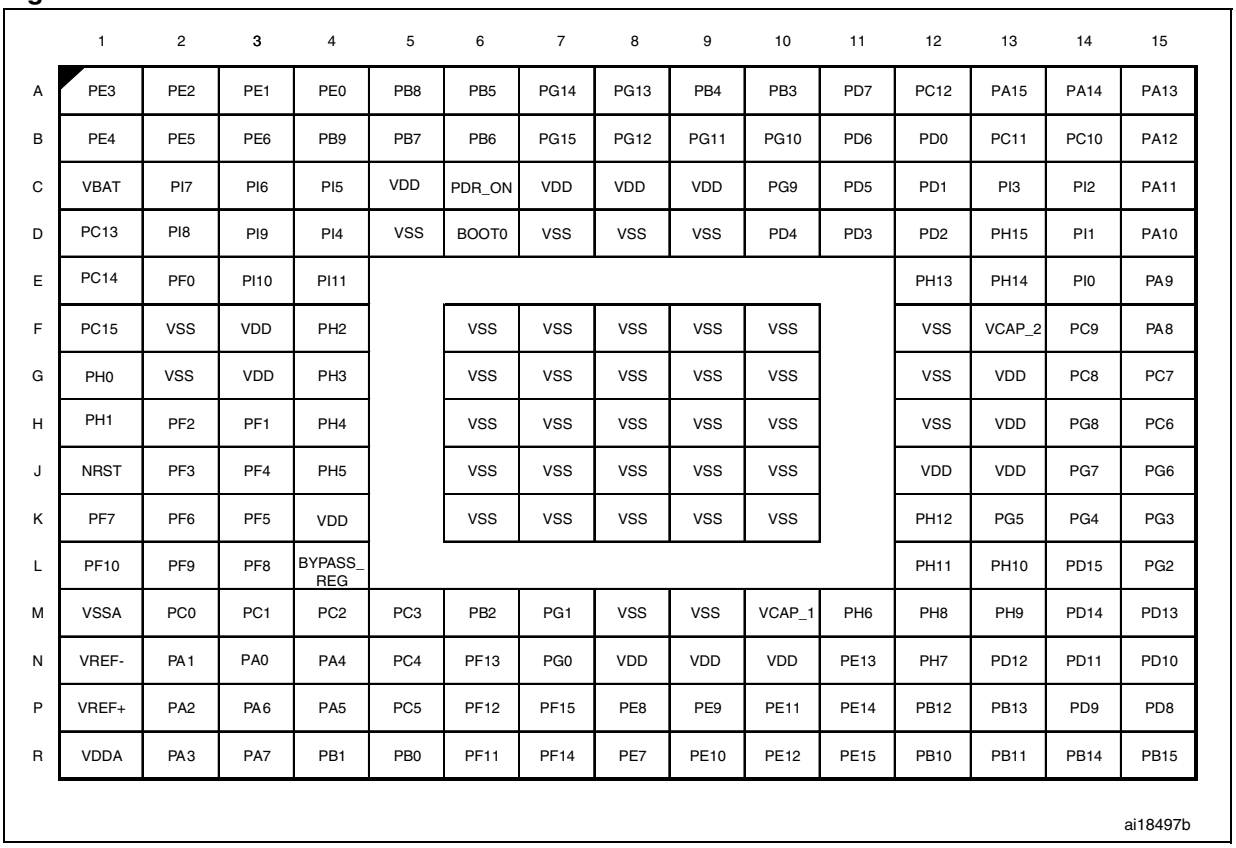


Figure 11. STM32F407GDIE UFBGA176 ballout



3.6 WLCSP90- 90-bump wafer level chip size package

Figure 12. Bonding diagram for WLCSP90

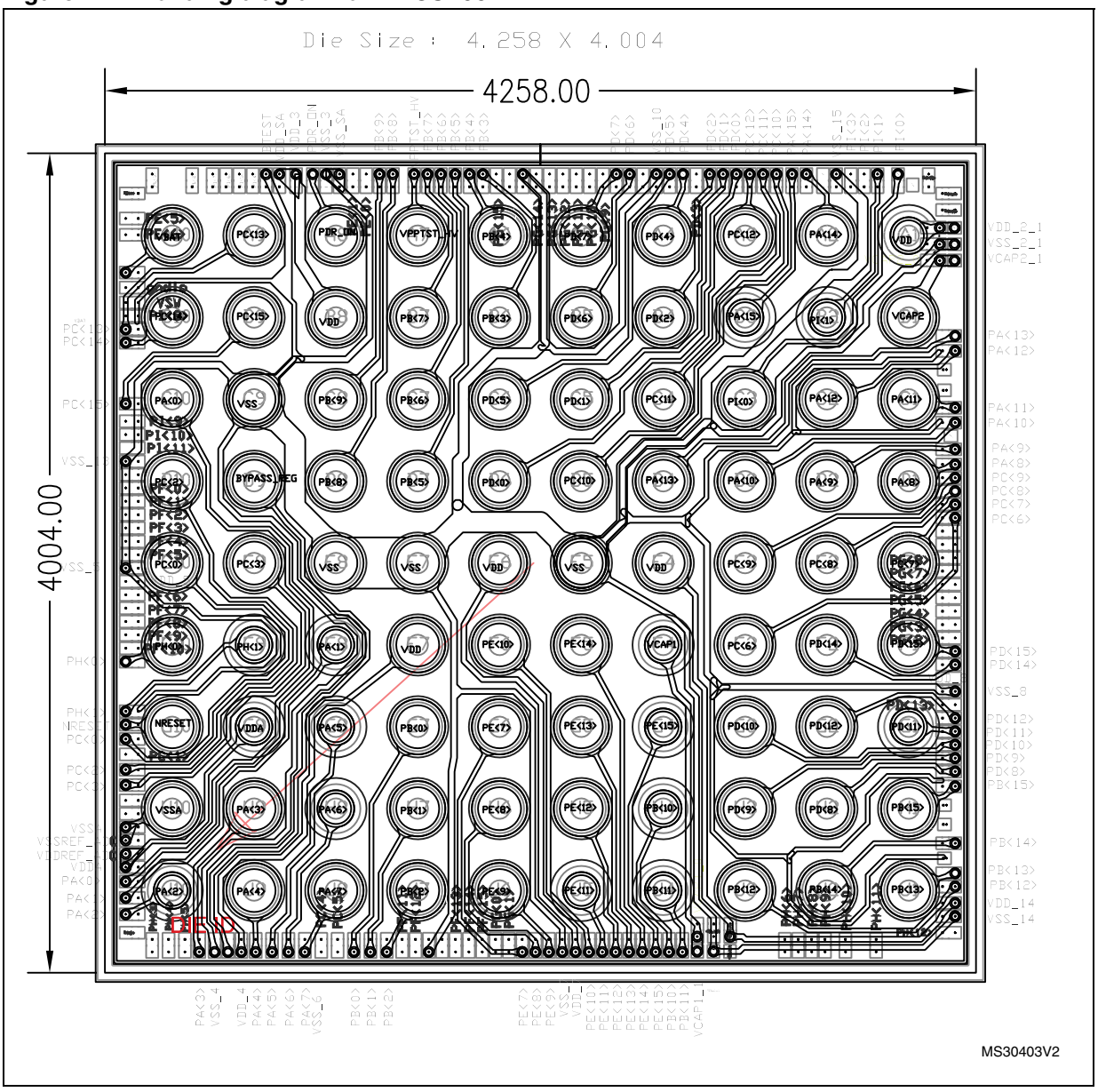
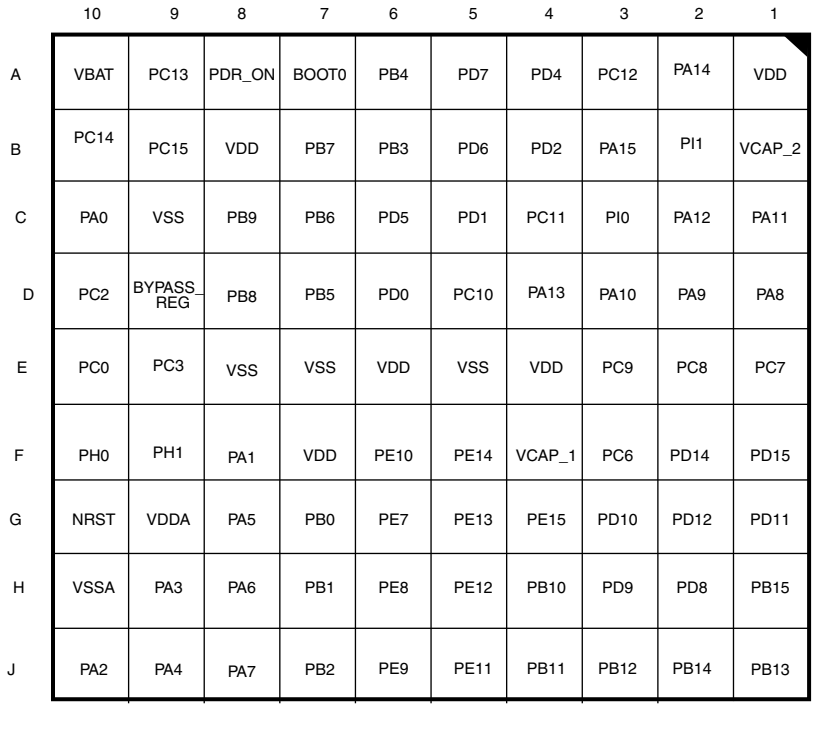


Figure 13. STM32F407GDIE WLCSP90 ballout



MS30402V1

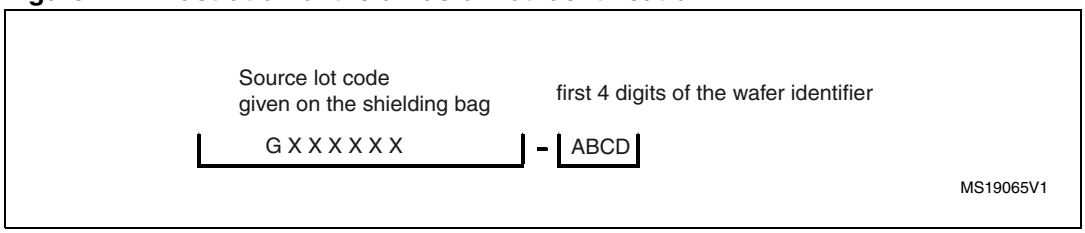
4 Diffusion lot identification

The lot is identified by the “source lot” numbers plus the first 4 digits (ABCD) of the wafer identifier (see *Figure 14*) where:

AB is the wafer number

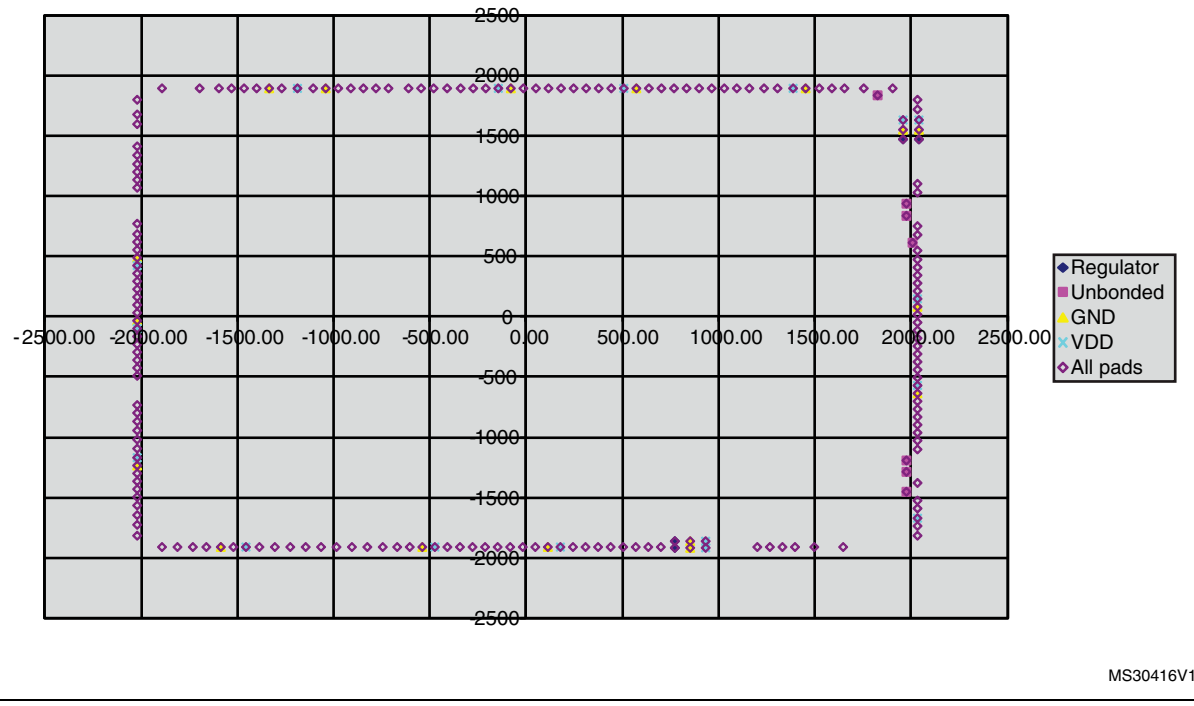
CD is the checksum of the diffusion lot identifier as specified in the SEMI M12-92 standard.

Figure 14. Illustration of the diffusion lot identification



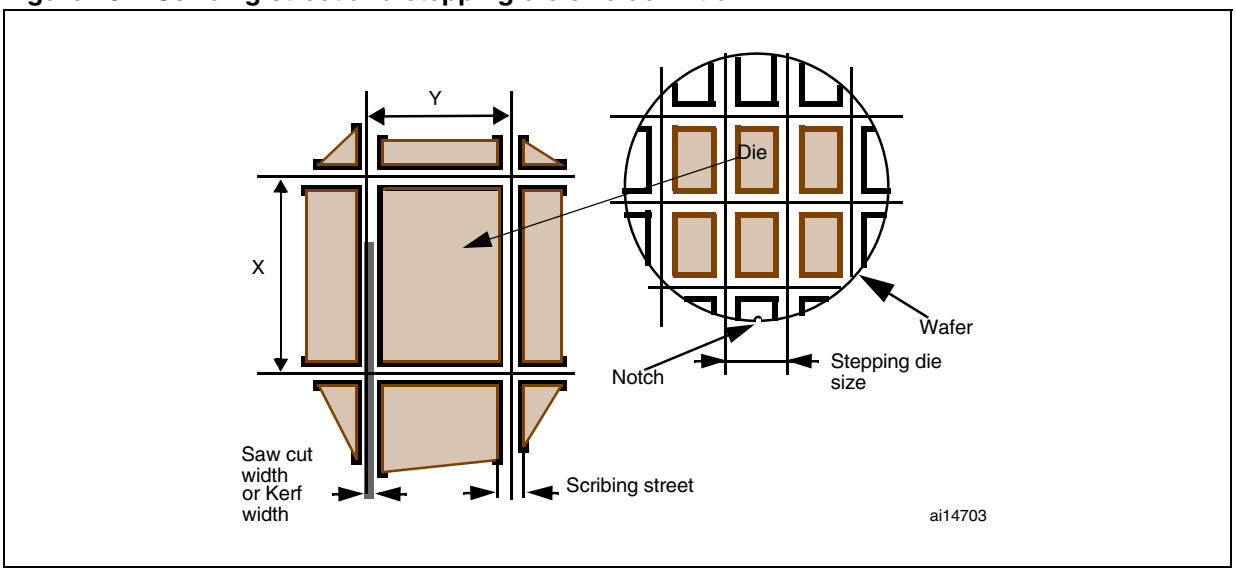
5 Die layout

Figure 15. Pad position and power bonding



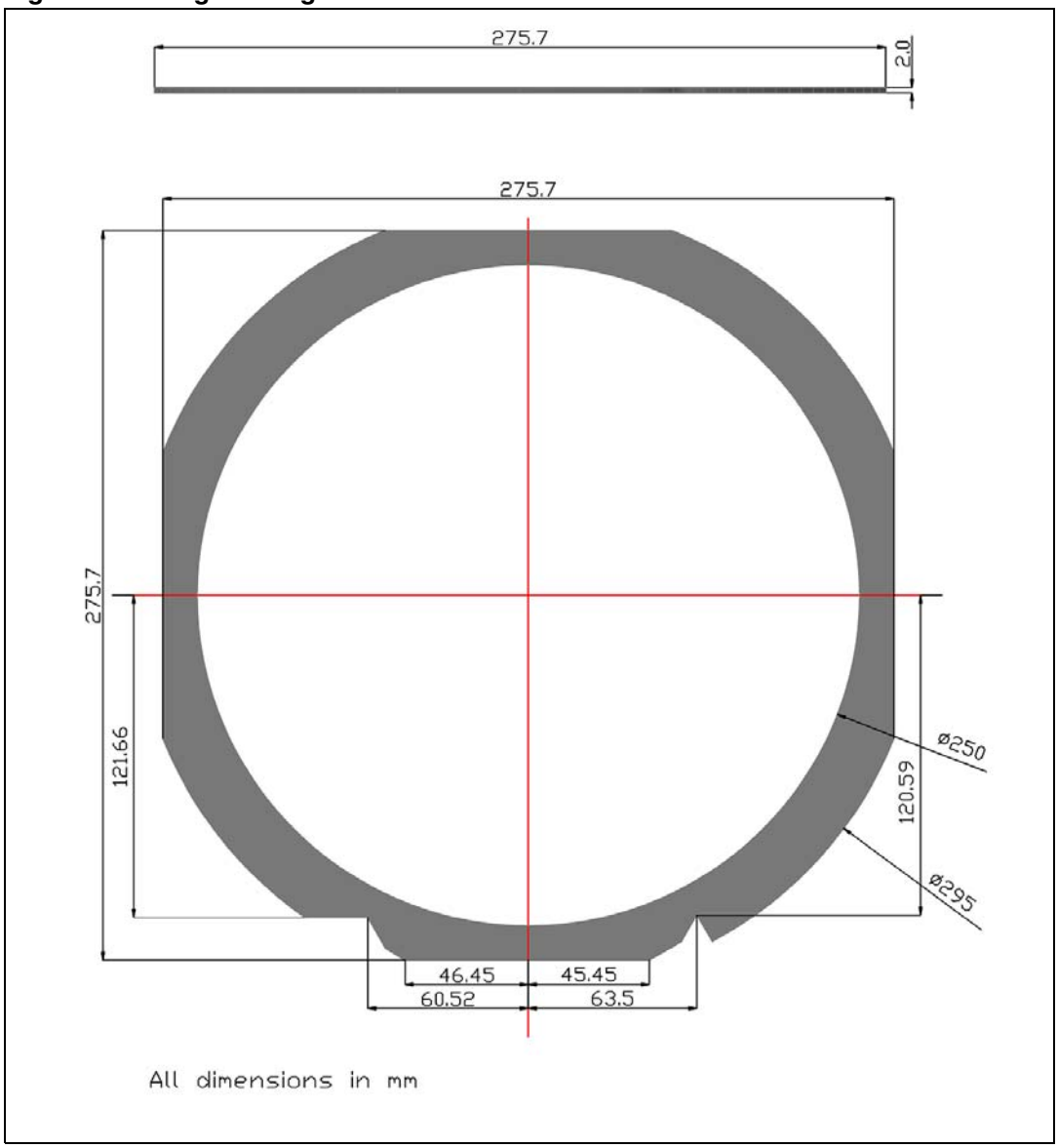
1. For power bonding recomendations, refer to *Section 3: Bonding diagrams and pinout/ballout schematics*.
2. Refer to *Table 6* for the correlation between pad number and pad name.

Figure 16. Scribing street and stepping die size definition



1. For power bonding recomendations, refer to *Section 3: Bonding diagrams and pinout/ballout schematics*.

Figure 17. Ring drawing for 8” wafer



6 Pad coordinates

In *Table 6*, all dimensions are given in µm. Pad position values correspond to the distance between the center of the die and the center of the pad bonding area (see *Figure 18: Pad schematics (all pads except NC pins)*).

Table 6. Pad coordinates

Signal name	Pad number	Pad position(1)		Pad dimension	
		X(µm)	Y(µm)	X(µm)	Y(µm)
PE4	1	–2027.05	1805.58	123	59
PE5	2	–2027.05	1683.79	123	59
PE6	3	–2027.05	1603.7	123	59
VBAT	4	–2027.05	1419.32	123	59
NC	5	–2027.05	1346.04	123	59
NC	6	–2027.05	1272.74	123	59
PI8	7	–2027.05	1207.51	123	59
PC13	8	–2027.05	1142.27	123	59
PC14	9	–2027.05	1077.03	123	59
PC15	10	–2027.05	778.54	123	59
PI9	11	–2027.05	692.59	123	59
PI10	12	–2027.05	627.34	123	59
PI11	13	–2027.05	562.1	123	59
VSS	14	–2027.05	496.93	123	59
VDD	15	–2027.05	431.83	123	59
PF0	16	–2027.05	366.67	123	59
PF1	17	–2027.05	301.42	123	59
PF2	18	–2027.05	236.18	123	59
PF3	19	–2027.05	170.94	123	59
PF4	20	–2027.05	105.7	123	59
PF5	21	–2027.05	40.46	123	59
VSS	22	–2027.05	–24.78	123	59
VDD	23	–2027.05	–90.01	123	59
PF6	24	–2027.05	–155.26	123	59
PF7	25	–2027.05	–220.49	123	59
PF8	26	–2027.05	–285.73	123	59
PF9	27	–2027.05	–350.98	123	59
PF10	28	–2027.05	–416.21	123	59

Table 6. Pad coordinates (continued)

Signal name	Pad number	Pad position(1)		Pad dimension	
		X(µm)	Y(µm)	X(µm)	Y(µm)
PH0	29	–2027.05	–481.45	123	59
PH1	30	–2027.05	–724.22	123	59
NRST	31	–2027.05	–789.46	123	59
PC0	32	–2027.05	–859.59	123	59
PC1	33	–2027.05	–934.64	123	59
PC2	34	–2027.05	–1009.68	123	59
PC3	35	–2027.05	–1084.71	123	59
VDD	36	–2027.05	–1159.82	123	59
VSS	37	–2027.05	–1224.93	123	59
VSSA	38	–2027.05	–1290.09	123	59
V_{REF-}	39	–2027.05	–1355.32	123	59
V_{REF+}	40	–2027.05	–1420.57	123	59
VDDA	41	–2027.05	–1485.81	123	59
PA0	42	–2027.05	–1555.95	123	59
PA1	43	–2027.05	–1636.04	123	59
PA2	44	–2027.05	–1716.11	123	59
PH2	45	–2027.05	–1806.14	123	59
PH3	46	–1897.97	–1900.21	59	123
PH4	47	–1817.90	–1900.21	59	123
PH5	48	–1737.81	–1900.21	59	123
PA3	49	–1667.68	–1900.21	59	123
VSS	50	–1592.49	–1900.21	59	123
BYPASS_REG	51	–1527.25	–1900.21	59	123
VDD	52	–1462.02	–1900.21	59	123
PA4	53	–1391.88	–1900.21	59	123
PA5	54	–1311.80	–1900.21	59	123
PA6	55	–1231.71	–1900.21	59	123
PA7	56	–1151.64	–1900.21	59	123
PC4	57	–1071.56	–1900.21	59	123
PC5	58	–991.47	–1900.21	59	123
PB0	59	–911.40	–1900.21	59	123
PB1	60	–831.32	–1900.21	59	123
PB2	61	–751.23	–1900.21	59	123

Table 6. Pad coordinates (continued)

Signal name	Pad number	Pad position(1)		Pad dimension	
		X(µm)	Y(µm)	X(µm)	Y(µm)
PF11	62	–676.05	–1900.21	59	123
PF12	63	–610.82	–1900.21	59	123
VSS	64	–545.65	–1900.21	59	123
VDD	65	–480.55	–1900.21	59	123
PF13	66	–415.38	–1900.21	59	123
PF14	67	–350.14	–1900.21	59	123
PF15	68	–284.89	–1900.21	59	123
PG0	69	–219.65	–1900.21	59	123
PG1	70	–154.41	–1900.21	59	123
PE7	71	–89.18	–1900.21	59	123
PE8	72	–23.94	–1900.21	59	123
PE9	73	41.31	–1900.21	59	123
VSS	74	106.54	–1900.21	59	123
VDD	75	171.79	–1900.21	59	123
PE10	76	237.02	–1900.21	59	123
PE11	77	302.27	–1900.21	59	123
PE12	78	367.51	–1900.21	59	123
PE13	79	432.74	–1900.21	59	123
PE14	80	497.98	–1900.21	59	123
PE15	81	563.22	–1900.21	59	123
PB10	82	628.47	–1900.21	59	123
PB11	83	693.71	–1900.21	59	123
VCAP1_0	84	766.36	–1852.21	59	65
VCAP1_1	85	766.36	–1907.21	59	65
VSS_1_0	86	846.09	–1852.21	59	65
VSS_1_1	87	846.09	–1907.21	59	65
VDD_1_0	88	926.53	–1852.21	59	65
VDD_1_1	89	926.53	–1907.21	59	65
PH6	90	1194.91	–1900.21	59	123
PH7	91	1260.15	–1900.21	59	123
PH8	92	1325.39	–1900.21	59	123
PH9	93	1390.63	–1900.21	59	123
PH10	94	1490.86	–1900.21	59	123

Table 6. Pad coordinates (continued)

Signal name	Pad number	Pad position(1)		Pad dimension	
		X(µm)	Y(µm)	X(µm)	Y(µm)
PH11	95	1640.94	–1900.21	59	123
PH12	96	2027.06	–1806.14	123	59
VSS	97	2027.06	–1726.13	123	59
VDD	98	2027.06	–1661.03	123	59
PB12	99	2027.06	–1580.73	123	59
PB13	100	2027.06	–1515.49	123	59
VDD 12(2)		1969.63	–1442.36	-	-
PB14	101	2027.06	–1369.23	123	59
VDD 12(2)		1969.63	–1277.23	-	-
VDD 12(2)		1969.63	–1183.11	-	-
PB15	102	2027.06	–1091.11	123	59
PD8	103	2027.06	–1018.49	123	59
PD9	104	2027.06	–953.26	123	59
PD10	105	2027.06	–888.02	123	59
PD11	106	2027.06	–822.78	123	59
PD12	107	2027.06	–757.53	123	59
PD13	108	2027.06	–692.29	123	59
VSS	109	2027.06	–627.13	123	59
VDD	110	2027.06	–562.03	123	59
PD14	111	2027.06	–496.58	123	59
PD15	112	2027.06	–431.33	123	59
PG2	113	2027.06	–366.1	123	59
PG3	114	2027.06	–300.86	123	59
PG4	115	2027.06	–235.61	123	59
PG5	116	2027.06	–170.38	123	59
PG6	117	2027.06	–105.13	123	59
PG7	118	2027.06	–39.89	123	59
PG8	119	2027.06	25.34	123	59
VSS	120	2027.06	90.51	123	59
VDD	121	2027.06	155.62	123	59
PC6	122	2027.06	220.79	123	59
PC7	123	2027.06	286.02	123	59
PC8	124	2027.06	351.27	123	59

Table 6. Pad coordinates (continued)

Signal name	Pad number	Pad position(1)		Pad dimension	
		X(µm)	Y(µm)	X(µm)	Y(µm)
PC9	125	2027.06	416.51	123	59
PA8	126	2027.06	481.74	123	59
PA9	127	2027.06	555.95	123	59
VDD 12(2)		2001.47	621.08	-	-
PA10	128	2027.06	686.15	123	59
PA11	129	2027.06	758.77	123	59
VDD 12(2)		1969.63	844.08	-	-
VDD 12(2)		1969.63	944.89	-	-
PA12	130	2027.06	1036.89	123	59
PA13	131	2027.06	1109.51	123	59
VCAP2_1	132	2034.56	1477.84	65	59
VCAP2_0	133	1952.06	1477.84	65	59
VSS_2_1	134	2034.56	1557.56	65	59
VSS_2_0	135	1952.06	1557.56	65	59
VDD_2_1	136	2034.56	1638.01	65	59
VDD_2_0	137	1952.06	1638.01	65	59
PH13	138	2027.06	1725.51	123	59
PH14	139	2027.06	1805.58	123	59
PH15	140	1897.98	1900.22	59	123
VDD 12(2)		1819.78	1842.29	-	-
PI0	141	1747.91	1900.22	59	123
PI1	142	1647.67	1900.22	59	123
PI2	143	1582.43	1900.22	59	123
PI3	144	1516.91	1900.22	59	123
VSS	145	1445.85	1900.22	59	123
VDD	146	1380.76	1900.22	59	123
PA14	147	1299.91	1900.22	59	123
PA15	148	1229.77	1900.22	59	123
PC10	149	1153.46	1900.22	59	123
PC11	150	1088.22	1900.22	59	123
PC12	151	1022.98	1900.22	59	123
PD0	152	957.74	1900.22	59	123
PD1	153	892.51	1900.22	59	123

Table 6. Pad coordinates (continued)

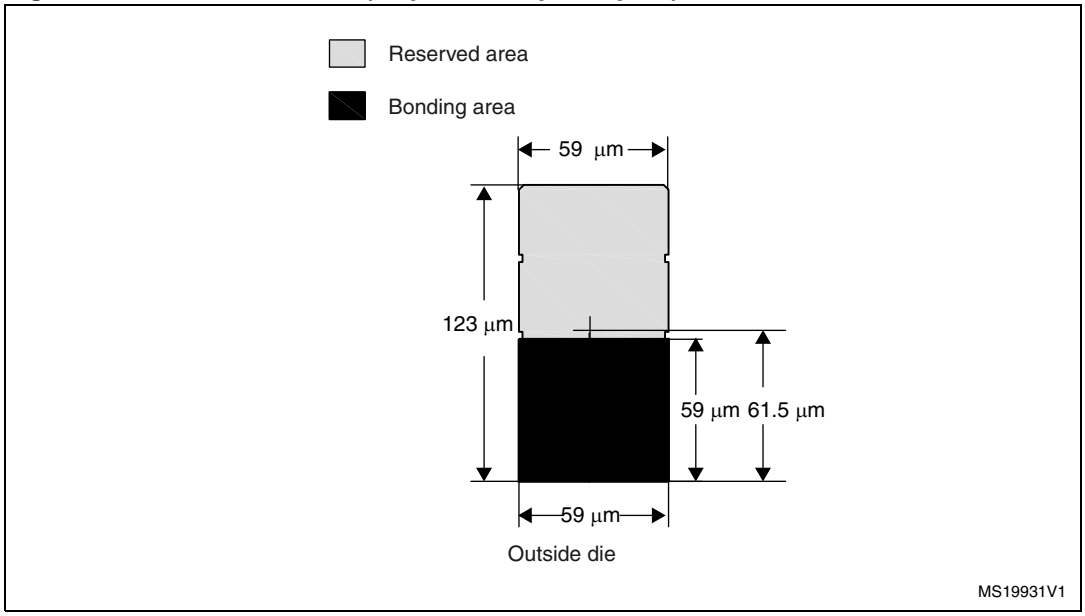
Signal name	Pad number	Pad position(1)		Pad dimension	
		X(µm)	Y(µm)	X(µm)	Y(µm)
PD2	154	827.27	1900.22	59	123
PD3	155	762.03	1900.22	59	123
PD4	156	696.78	1900.22	59	123
PD5	157	631.54	1900.22	59	123
VSS	158	566.38	1900.22	59	123
VDD	159	501.28	1900.22	59	123
PD6	160	436.11	1900.22	59	123
PD7	161	370.86	1900.22	59	123
PG9	162	305.63	1900.22	59	123
PG10	163	240.39	1900.22	59	123
PG11	164	175.15	1900.22	59	123
PG12	165	109.90	1900.22	59	123
PG13	166	44.66	1900.22	59	123
PG14	167	–20.58	1900.22	59	123
VSS	168	–85.75	1900.22	59	123
VDD	169	–150.85	1900.22	59	123
PG15	170	–216.01	1900.22	59	123
PB3	171	–281.26	1900.22	59	123
PB4	172	–346.49	1900.22	59	123
PB5	173	–416.64	1900.22	59	123
PB6	174	–486.78	1900.22	59	123
PB7	175	–552.02	1900.22	59	123
BOOT0	176	–617.26	1900.22	59	123
PB8	177	–721.41	1900.22	59	123
PB9	178	–786.66	1900.22	59	123
PE0	179	–851.90	1900.22	59	123
PE1	180	–917.14	1900.22	59	123
VSSA	181	–982.38	1900.22	59	123
VSS_3	182	–1047.61	1900.22	59	123
PDR_ON	183	–1112.85	1900.22	59	123
VDD	184	–1194.47	1900.22	59	123
VDDA	185	–1276.09	1900.22	59	123
VSS	186	–1341.31	1900.22	59	123

Table 6. Pad coordinates (continued)

Signal name	Pad number	Pad position(1)		Pad dimension	
		X(µm)	Y(µm)	X(µm)	Y(µm)
PI4	187	–1406.57	1900.22	59	123
PI5	188	–1471.81	1900.22	59	123
PI6	189	–1537.06	1900.22	59	123
PI7	190	–1602.30	1900.22	59	123
PE2	191	–1702.54	1900.22	59	123
PE3	192	–1897.97	1900.22	59	123

1. These coordinates are given from the center of the bounding area to the center of the die.
2. This pad must be left unbounded.

Figure 18. Pad schematics (all pads except NC pins)



1. Pads dimensions are expressed in µm.

7 Specific warning for die handling

7.1 Assembly qualification

Due to lower silicon rate in resin (percentage of silica in the mold compound) compared to plastic package, the COB (chip on board) assembly could be more sensitive to delamination.

Assembly reliability: as the assembly process is a key factor for module reliability, STMicroelectronics requires that the module is fully qualified, according to industry-standard quality requirements.

For instance:

- Thermal cycles: 2000 cycles, –40 °C/+150 °C
- Temperature and humidity: 85°C, 85%RH
- Construction analysis
- Process and equipment FMEA's / control plan
- Process flow / SPC capability

Running temperature extraction by resin must be checked as thermal resistance given for STMicroelectronics packages cannot be applied.

7.2 Traceability

ST requires a marking of the diffusion lot number and wafer number on the module for full traceability. This can be done directly on the PCB after assembly.

ST requires that the customer has his own traceability marking and a system with a full proof crosslink between the ST diffusion lot number and module number until delivery to the end customer.

7.3 Failure analysis

Failure analysis is done only if the reject rate reaches a 0.5% threshold.

Normally STMicroelectronics is not able to perform electrical retesting on dice, however electrical tests can be run if the customer fulfills the following requirements:

- End customer returns are first confirmed on the ST customer's manufacturing test equipment (ST requires a full application test coverage versus end customer application. ST declines responsibility for failures detected by end customers and not screened by ST customer production test).
- "Double pad implementation" is required (a specific layout on the application equivalent to the footprint of a standard JEDEC package taken from an equivalent package product). This allows the sawing of the application for failure analysis retesting in standard socketed equipment. For NVM failure analysis, a JTAG connection is a minimum requirement.

In addition, if the part is found good on ST's automatic test equipment (ATE), a method to replug the device into a reference module for further investigations is needed.

The customer must have the ability to remove the resin that covers the die (and keeps the application functional), making it possible to access all the die connections on the PCB side to allow probing if needed (contacts on PCB must be free of resin and varnish). This must be followed by visual inspection and continuity checking by the customer or assembly subcontractor.

Please contact your sales office for additional information, as before any failure analysis, STMicroelectronics will make a feasibility study for evaluation, which may lead to financial participation in some cases.

7.4 Flash memory recommendations

Retention guarantee is the same as for the assembled product. Special care must be taken due to sensitivity to UV exposure (refer to paragraph below).

Non-volatile memories (NVM) contain reference cells made of NVM cells and the system boot Flash, which are programmed during test at ST. If a die is exposed to UV light with sufficient intensity and duration, these cells could be corrupted. This corruption can induce nonfunctionality of the entire memory just after the exposure or reduce the retention performance. In order to prevent corruption from occurring, special care must be taken to protect the die from long UV exposure.

For example:

- Assembly process can be critical, some plasma used for cleaning processes are known to generate UV light. Contact your plasma supplier for details
- PCB and glob top resin opacity to UV must be checked
- Extended storage in non-UV opaque packing

Normal neon light exposure during standard assembly process is sustainable without impact on retention.

7.5 Unbounded pads

Floating I/Os can be managed by software by activating each I/O internal weak pull-up/pull-down individually.

7.6 Minimum power bonding requirements

7.6.1 Power supply pads

The following pads **must** be bonded to V_{DD}:

- All VDD pads
- VDDA, V_{REF+}

The following pads **must** be bonded to GND:

- All VSS pads
- VSSA, VREF-

7.7 Regulator pads

The pads listed below must be bonded as follows:

- All VCAP1_x **must** be bonded to an external capacitor C1 = 2.2 µF
- All VCAP2_x **must** be bonded to an external capacitor C2 = 2.2 µF

7.7.1 PDR_ON pad

The PDR_On pad must be managed as described in the product datasheet. It can be either connected to V_{DD} or V_{SS}.

7.7.2 REGOFF pad

This REGOFF pad **must** be managed as described in the product datasheet. It can be either connected to V_{DD} or V_{SS}.

7.7.3 NC pads

The NC pads must be left unconnected.

7.8 Guarantee

With the above considerations, it is clear that the final guarantee of the microcontroller inside the application is shared between the customer and ST.

It is understood by customers that STMicroelectronics delivers parts screened at wafer level, therefore few rejects are expected to be found during the final screening after mounting.

STMicroelectronics will not endorse responsibility for those rejects below the maximum threshold of 0.5%.

8 Revision history

Table 7. Document revision history

Date	Revision	Changes
19-Apr-2012	1	Initial release.
29-Jun-2012	2	Updated *Figure 12: Bonding diagram for WLCSP90*. Removed references to VDD_SA, VDD_1_0, VDD_1_1, VDD_2_0, VDD_2_1. VSS_1_0, VSS_1_1, VSS_2_0, and VSS_2_1 in *Section 7.6.1: Power supply pads* and *Section 7.7: Regulator pads*. VCAP1_0/1 and VCAP2_0/1 replaced by VCAP1_x and VCAP2_x in *Section 7.7: Regulator pads*.

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