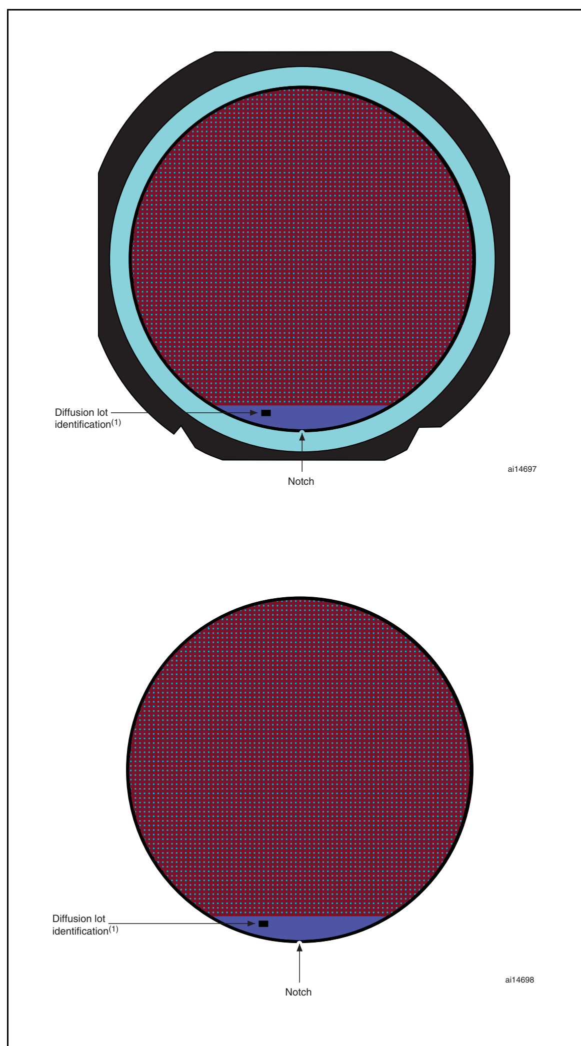
STM32F103EDIE

High-density STM32F103xx die specification

Data brief

Features

- Wafer size: 8 inches
- Die identification: T414A
- Die stepping (X,Y): 4511, 4440 µm
- Wafer thickness: 381 ± 25 µm
- Scribe street (X,Y): 80, 80 µm
- Die finish front side: polyimide
- Die finish back side: raw silicon
- Wafer type (Si, GaAs, Others): Si
- Process type: CMOS
- Pad number per die: 154
- Laser trimming: not applicable



1. For the Diffusion lot identification, refer to *Diffusion lot identification on page 13*.

For further information contact your local STMicroelectronics sales office. www.st.com

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1 Die description

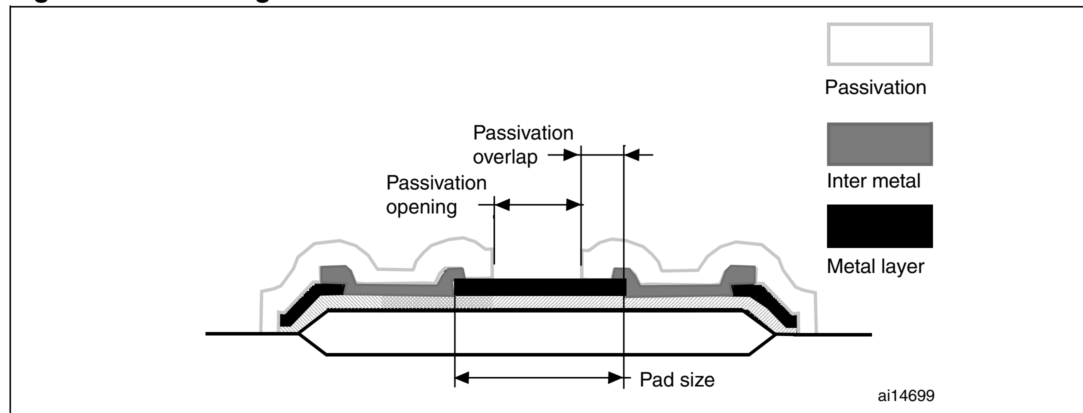
Important note: Refer to *Section 4* for specific handling terms and conditions.

Table 1. Wire bond pad metal

Wire bond pad metal	Composition	Thickness (µm)
Metal 1	Tin/AlCu/Tin	0.45
Metal 2	Tin/AlCu/Tin	0.45
Metal 3	Tin/AlCu/Tin	0.45
Metal 4	Tin/AlCu/Tin	0.45
Metal 5	Tin/AlCu/Tin	0.875

I/O type: CUP (circuit under pad).

Figure 1. Pad diagram



Pad size X = 75 µm, Y = 80 µm

Passivation opening X = 65 µm, Y = 70 µm

Minimum passivation and pad overlap 5 µm for one side

Table 2. Assembly features (critical dimensions)

Wire quantity	Wire material type	Wire diameter	Bond pad windows (X,Y)	Minimum pitch	Wire bond pad placement
N/A	N/A	25 µm	65.70 µm	80 µm	100%

1.1 Wafer processing and assembly

1.1.1 Good dice

The wafers are ink marked.
All dice which are not good are marked with an ink spot.

Number of chips per wafer	Gross chips:	1379
	Good chips:	> 1170 (85% on average)

1.1.2 Back-lapping

Back-lapping is permitted on these wafers to reduce wafer thickness. ST does not perform additional back-lapping in house for these products, it has to be done by a sub-contractor.

Minimum thickness allowed: 150 µm

1.1.3 Assembly

Please refer to the following package bonding and package pin-out for pad / pin relation.

The Autocad or GDS files of pad opening are available upon request:

GDS file

Autocad file

Figure 2. Bonding diagram for LQFP144

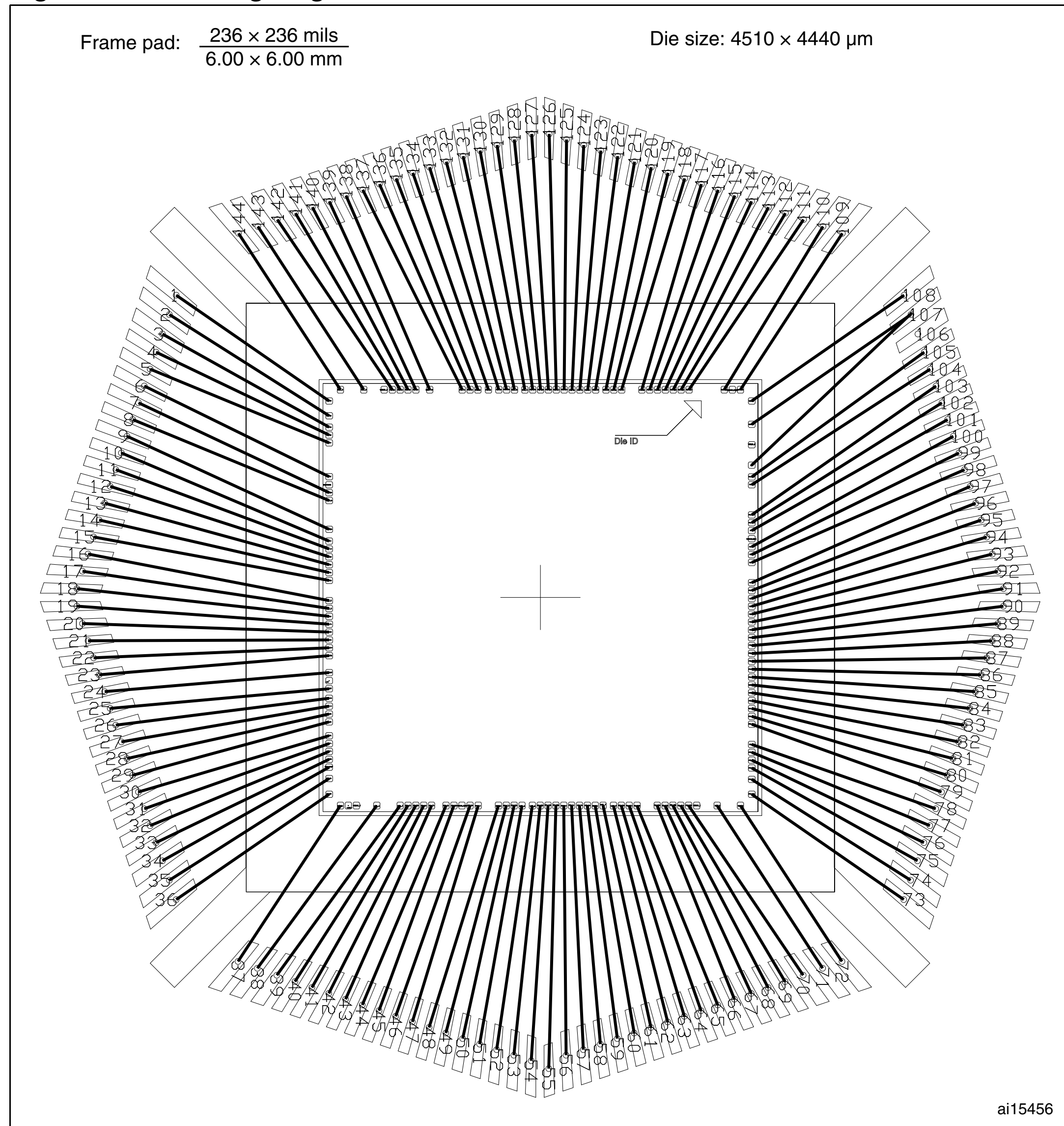


Figure 3. LQFP144 pinout

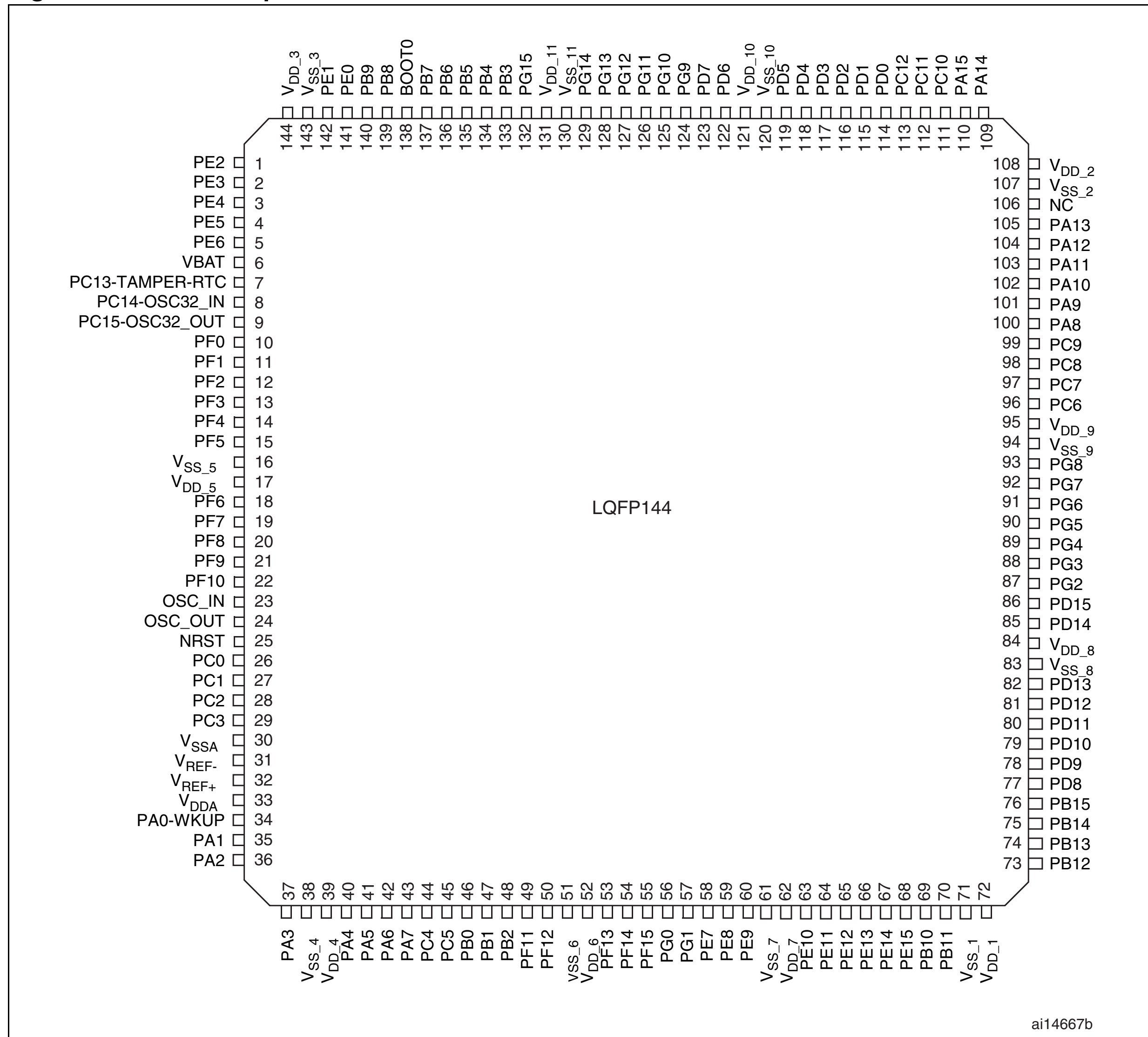


Figure 4. Bonding diagram for LQFP100

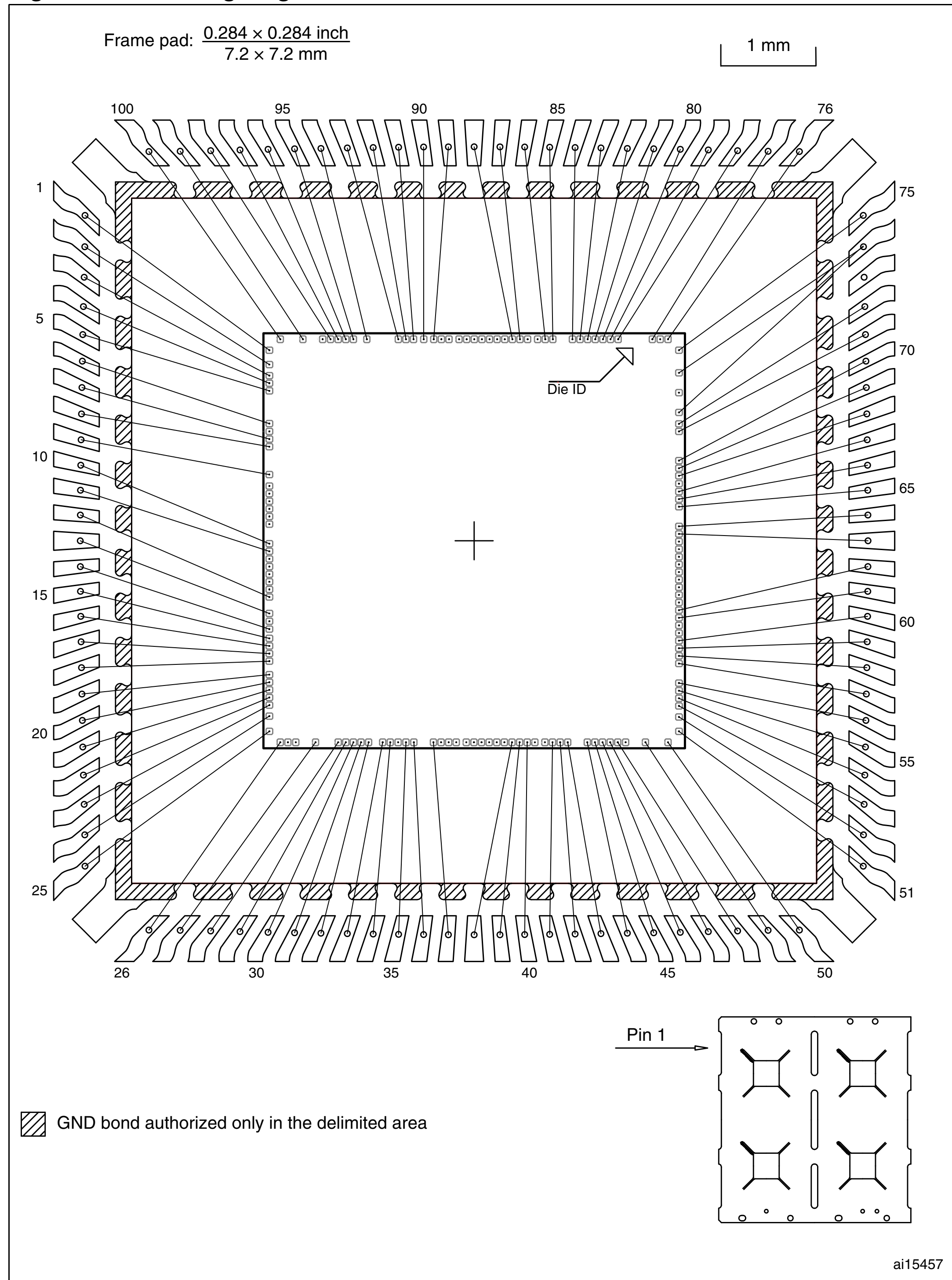
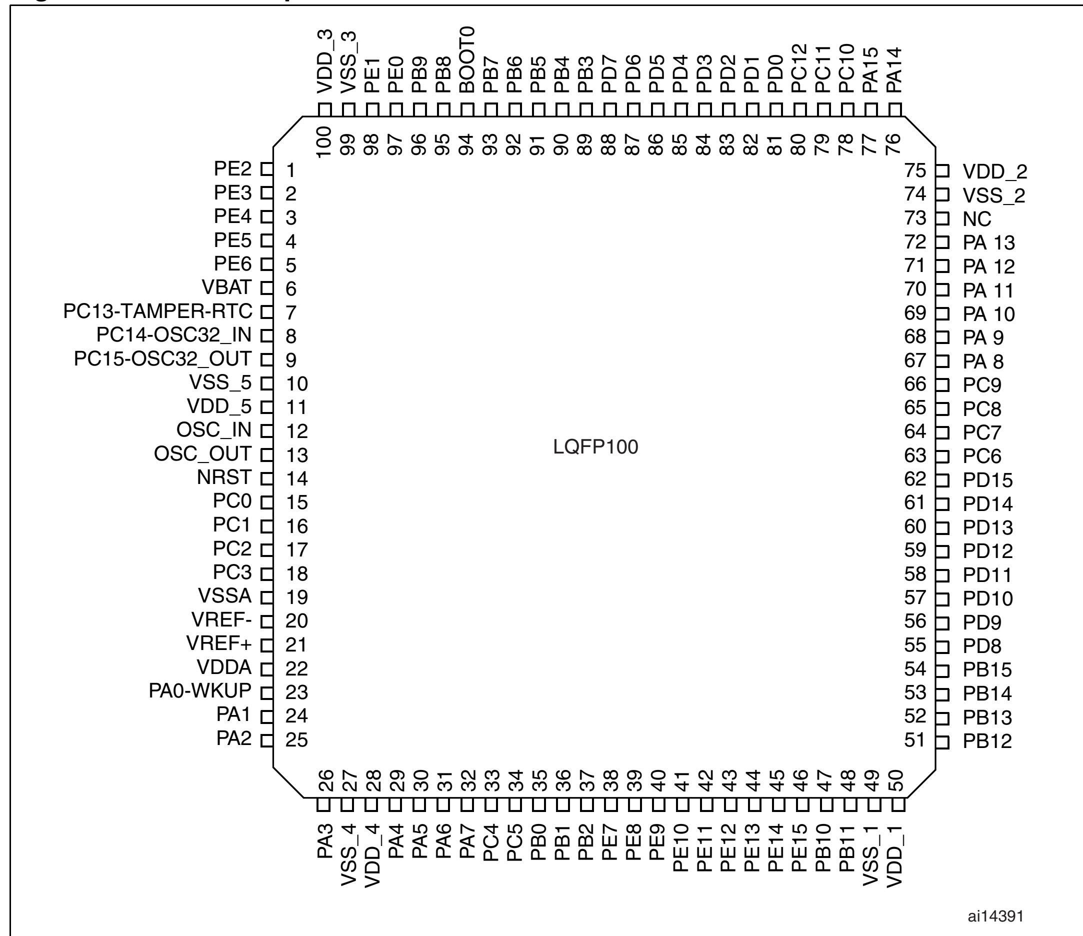


Figure 5. LQFP100 pinout



Warning: **The supported die is as follows: 512 KB on 144 pins, one bonding, one memory footprint. The application must configure by software the unused pins for bondings below 144 pins.**

Figure 6. Bonding diagram for LQFP64

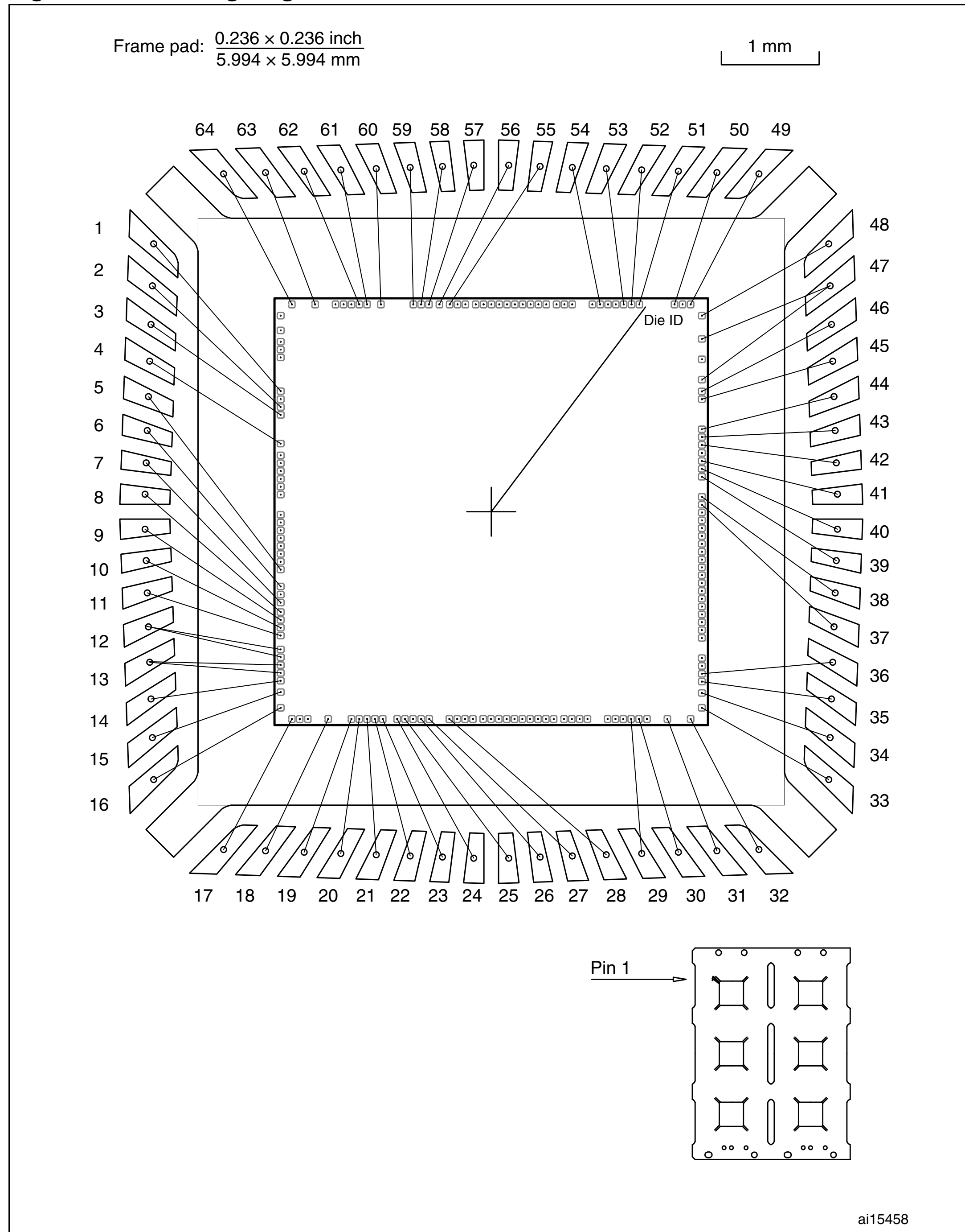
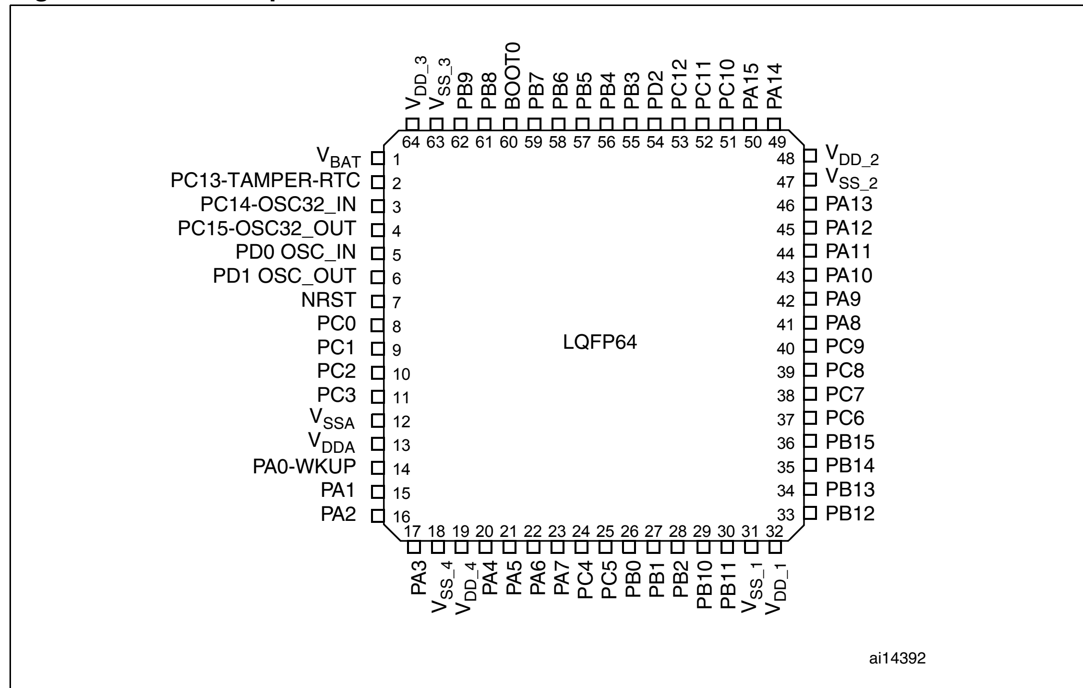


Figure 7. LQFP64 pinout



Warning: The supported die is as follows: 512 KB on 144 pins, one bonding, one memory footprint. The application must configure by software the unused pins for bondings below 144 pins.

1.2 Ordering information

Table 3. Ordering information

Die part number	Sales type	Temperature range	Equivalent packaged part	Flash program memory (Kbytes)	SRAM memory (Kbytes)	Number of pins
STM32F103EDIE	STM32F103EDIE1	–40 °C to +85 °C	STM32F103ZET6	512	64	144

Note: For electrical and functional information, please refer to the datasheet and reference manual of the equivalent packaged part. The electrical characteristics are the same, with a restricted temperature range, except for a few parameters.
The values that change are specified in Table 4 below. For other characteristics, please refer to the high-density STM32F103xCDE datasheet available from the STMicroelectronics website: www.st.com.

Table 4. HSI oscillator accuracy(1) (2)

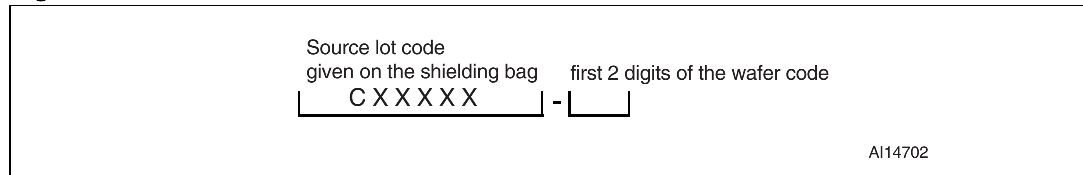
Symbol	Parameter	Conditions	Max	Unit
ACC_{HSI}	Accuracy of HSI oscillator	T_A = –40 to 85 °C	±3.5	%

1. Guaranteed by design, not tested in production.
2. V_{DD} = 3.3 V.

1.2.1 Diffusion lot identification

The lot is identified by the “source lot” numbers and the first 2 digits of the wafer code as shown below.

Figure 8. Illustration of the diffusion lot identification



2 Die layout

Figure 9. Die layout / notch position

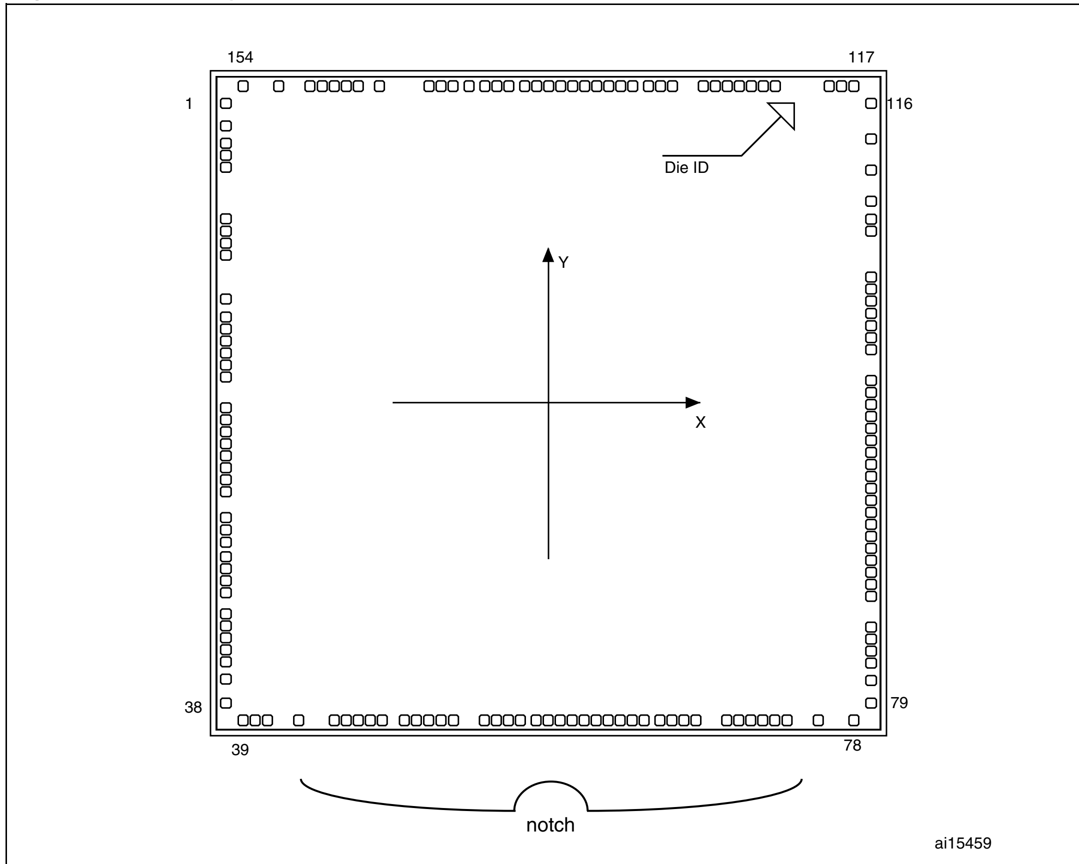


Figure 10. Scribing street and stepping die size definition

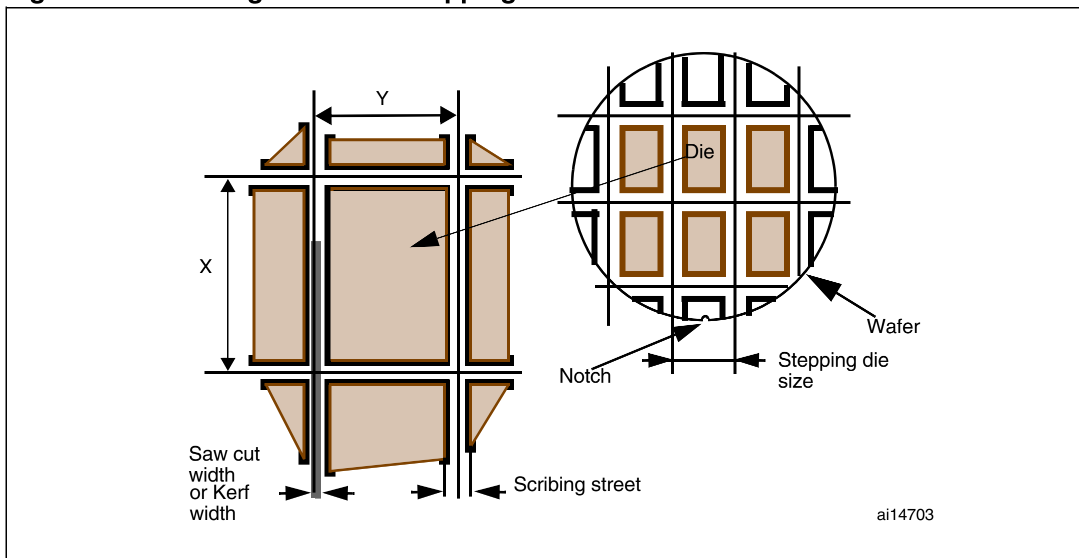
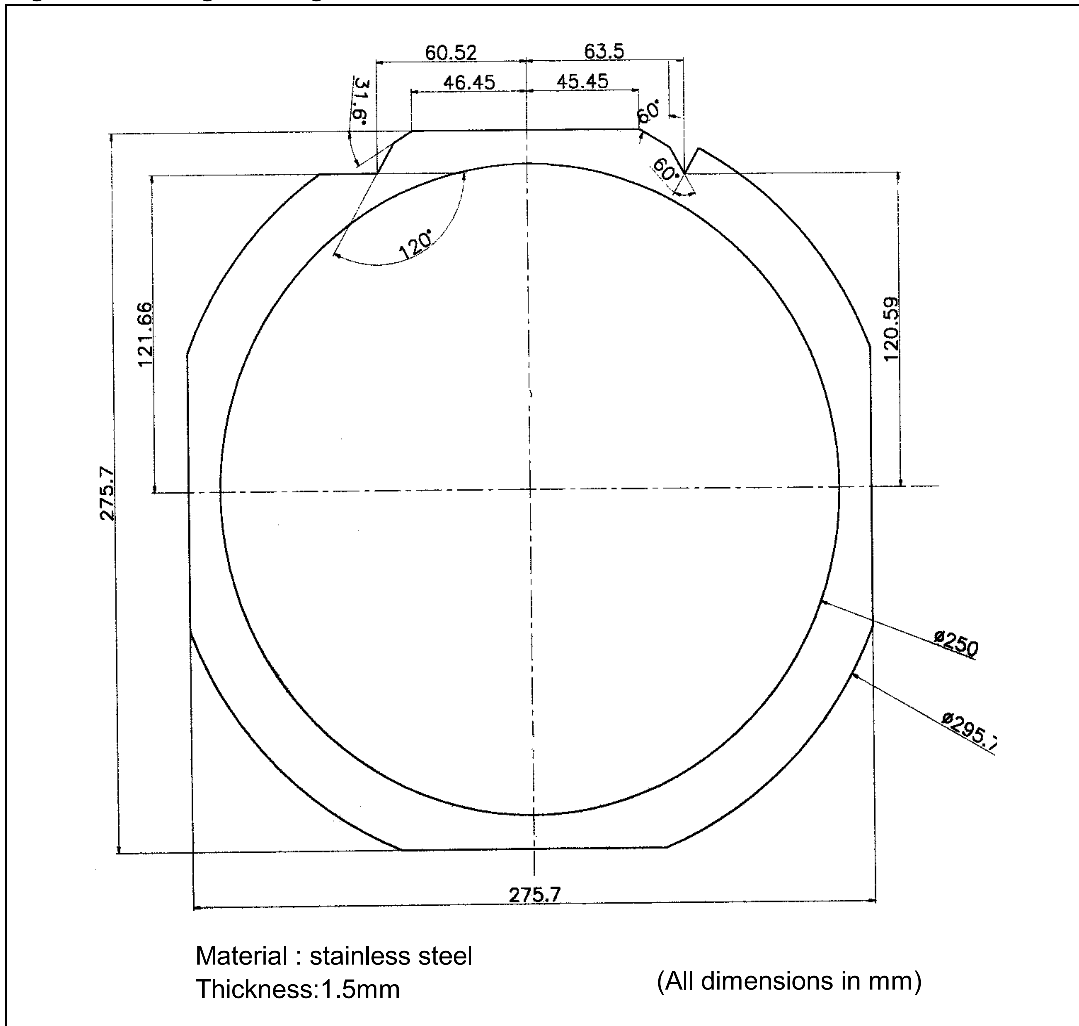


Figure 11. Ring drawing for 8” wafer



3 Pad coordinates

In *Table 5*, all dimensions are given in µm. Pad position values correspond to pad center coordinates. The origin is in the center of the die. The pad dimensions are 70 µm (length) × 65 µm (width = die side).

Warning: The supported die is as follows: 512 KB on 144 pins, one bonding, one memory footprint. The application must configure the unused pins for bondings below 144 pins.

Table 5. Pad coordinates

Pad No.	Pad name	144 pins		100 pins		64 pins		Pad position	
		Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	X	Y
1	PE2	1	PE2	1	PE2	-		-2152.6	2002.3
2	PE3	2	PE3	2	PE3	-		-2152.6	1851.7
3	PE4	3	PE4	3	PE4	-		-2152.6	1735.8
4	PE5	4	PE5	4	PE5	-		-2152.6	1655.7
5	PE6	5	PE6	5	PE6	-		-2152.6	1575.6
6	V_{BAT}	6	V_{BAT}	6	V_{BAT}	1	V_{BAT}	-2152.6	1231.4
7	DNU(1)							-2152.6	1148.9
8	PC13	7	PC13-TAMPER-RTC	7	PC13-TAMPER-RTC	2	PC13-TAMPER-RTC	-2152.6	1068.8
9	PC14	8	PC14-OSC32_IN	8	PC14-OSC32_IN	3	PC14-OSC32_IN	-2152.6	988.72
10	PC15	9	PC15-OSC32_OUT	9	PC15-OSC32_OUT	4	PC15-OSC32_OUT	-2152.6	695.84
11	PF0	10	PF0	-		-		-2152.6	575.44
12	PF1	11	PF1	-		-		-2152.6	495.36
13	PF2	12	PF2	-		-		-2152.6	415.28
14	PF3	13	PF3	-		-		-2152.6	335.2
15	PF4	14	PF4	-		-		-2152.6	255.12
16	PF5	15	PF5	-		-		-2152.6	175.04
17	V_{SS_5}	16	V_{SS_5}	10	V_{SS_5}	-		-2152.6	-30.48
18	V_{DD_5}	17	V_{DD_5}	11	V_{DD_5}	-		-2152.6	-110.56
19	PF6	18	PF6	-		-		-2152.6	-190.72
20	PF7	19	PF7	-		-		-2152.6	-270.72
21	PF8	20	PF8	-		-		-2152.6	-350.88

Table 5. Pad coordinates (continued)

Pad No.	Pad name	144 pins		100 pins		64 pins		Pad position	
		Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	X	Y
22	PF9	21	PF9	-		-		-2152.6	-430.96
23	PF10	22	PF10	-		-		-2152.6	-511.04
24	OSC_IN	23	OSC_IN	12	OSC_IN	5	PD0-OSC_IN	-2152.6	-591.04
25	OSC_OUT	24	OSC_OUT	13	OSC_OUT	6	PD1-OSC_OUT	-2152.6	-763.52
26	DNU(1)							-2152.6	-845.94
27	NRST	25	NRST	14	NRST	7	NRST	-2152.6	-928.16
28	PC0	26	PC0	15	PC0	8	PC0	-2152.6	-1025.1
29	PC1	27	PC1	16	PC1	9	PC1	-2152.6	-1105.2
30	PC2	28	PC2	17	PC2	10	PC2	-2152.6	-1185.3
31	PC3	29	PC3	18	PC3	11	PC3	-2152.6	-1265.4
32	V_{SSA}	30	V_{SSA}	19	V_{SSA}	12	V_{SSA}	-2152.6	-1406.4
33	V_{REF-}	31	V_{REF-}	20	V_{REF-}	-	V_{SSA}	-2152.6	-1486.5
34	V_{REF+}	32	V_{REF+}	21	V_{REF+}	-	V_{DDA}	-2152.6	-1566.6
35	V_{DDA}	33	V_{DDA}	22	V_{DDA}	13	V_{DDA}	-2152.6	-1646.6
36	PA0-WKUP	34	PA0-WKUP	23	PA0-WKUP	14	PA0-WKUP	-2152.6	-1726.7
37	PA1	35	PA1	24	PA1	15	PA1	-2152.6	-1842.1
38	PA2	36	PA2	25	PA2	16	PA2	-2152.6	-2002.3
39	PA3	37	PA3	26	PA3	17	PA3	-2037.6	-2117.3
40	DNU(1)							-1957.4	-2117.3
41	DNU(1)							-1875.1	-2117.3
42	V_{SS_4}	38	V_{SS_4}	27	V_{SS_4}	18	V_{SS_4}	-1666.9	-2117.3
43	V_{DD_4}	39	V_{DD_4}	28	V_{DD_4}	19	V_{DD_4}	-1429.4	-2117.3
44	PA4	40	PA4	29	PA4	20	PA4	-1349.4	-2117.3
45	PA5	41	PA5	30	PA5	21	PA5	-1269.3	-2117.3
46	PA6	42	PA6	31	PA6	22	PA6	-1189.2	-2117.3
47	PA7	43	PA7	32	PA7	23	PA7	-1109.1	-2117.3
48	PC4	44	PC4	33	PC4	24	PC4	-961.84	-2117.3
49	PC5	45	PC5	34	PC5	25	PC5	-881.76	-2117.3
50	DNU(1)							-799.46	-2117.3
51	PB0	46	PB0	35	PB0	26	PB0	-717.04	-2117.3
52	PB1	47	PB1	36	PB1	27	PB1	-633.68	-2117.3
53	PB2	48	PB2	37	PB2	28	PB2	-428.16	-2117.3

Table 5. Pad coordinates (continued)

Pad No.	Pad name	144 pins		100 pins		64 pins		Pad position	
		Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	X	Y
54	PF11	49	PF11	-		-		-348	-2117.3
55	PF12	50	PF12	-		-		-268	-2117.3
56	V_{SS_6}	51	V_{SS_6}	-		-		-187.92	-2117.3
57	V_{DD_6}	52	V_{DD_6}	-		-		-82.64	-2117.3
58	PF13	53	PF13	-		-		-2.48	-2117.3
59	PF14	54	PF14	-		-		77.52	-2117.3
60	PF15	55	PF15	-		-		157.6	-2117.3
61	PG0	56	PG0	-		-		237.68	-2117.3
62	PG1	57	PG1	-		-		317.76	-2117.3
63	PE7	58	PE7	38	PE7	-		397.84	-2117.3
64	PE8	59	PE8	39	PE8	-		477.92	-2117.3
65	PE9	60	PE9	40	PE9	-		558	-2117.3
66	V_{SS_7}	61	V_{SS_7}	-		-		638.08	-2117.3
67	V_{DD_7}	62	V_{DD_7}	-		-		743.36	-2117.3
68	PE10	63	PE10	41	PE10	-		823.44	-2117.3
69	PE11	64	PE11	42	PE11	-		903.52	-2117.3
70	PE12	65	PE12	43	PE12	-		983.6	-2117.3
71	PE13	66	PE13	44	PE13	-		1189.1	-2117.3
72	PE14	67	PE14	45	PE14	-		1269.2	-2117.3
73	PE15	68	PE15	46	PE15	-		1349.3	-2117.3
74	PB10	69	PB10	47	PB10	29	PB10	1429.4	-2117.3
75	PB11	70	PB11	48	PB11	30	PB11	1509.4	-2117.3
76	DNU(1)							1591.9	-2117.3
77	V_{SS_1}	71	V_{SS_1}	49	V_{SS_1}	31	V_{SS_1}	1800.1	-2117.3
78	V_{DD_1}	72	V_{DD_1}	50	V_{DD_1}	32	V_{DD_1}	2037.6	-2117.3
79	PB12	73	PB12	51	PB12	33	PB12	2152.6	-2002.3
80	PB13	74	PB13	52	PB13	31	PB13	2152.6	-1851.1
81	PB14	75	PB14	53	PB14	35	PB14	2152.6	-1735.2
82	PB15	76	PB15	54	PB15	36	PB15	2152.6	-1655.1
83	PD8	77	PD8	55	PD8	-		2152.6	-1575
84	PD9	78	PD9	56	PD9	-		2152.6	-1495
85	PD10	79	PD10	57	PD10	-		2152.6	-1289.4
86	PD11	80	PD11	58	PD11	-		2152.6	-1209.4

Table 5. Pad coordinates (continued)

Pad No.	Pad name	144 pins		100 pins		64 pins		Pad position	
		Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	X	Y
87	PD12	81	PD12	59	PD12	-		2152.6	-1129.3
88	PD13	82	PD13	60	PD13	-		2152.6	-1049.2
89	V_{SS_8}	83	V_{SS_8}	-		-		2152.6	-969.12
90	V_{DD_8}	84	V_{DD_8}	-		-		2152.6	-889.04
91	PD14	85	PD14	61	PD14	-		2152.6	-808.96
92	PD15	86	PD15	62	PD15	-		2152.6	-728.88
93	PG2	87	PG2	-		-		2152.6	-648.8
94	PG3	88	PG3	-		-		2152.6	-568.72
95	PG4	89	PG4	-		-		2152.6	-488.64
96	PG5	90	PG5	-		-		2152.6	-408.56
97	PG6	91	PG6	-		-		2152.6	-328.48
98	PG7	92	PG7	-		-		2152.6	-248.4
99	PG8	93	PG8	-		-		2152.6	-168.32
100	V_{SS_9}	94	V_{SS_9}	-		-		2152.6	-88.24
101	V_{DD_9}	95	V_{DD_9}	-		-		2152.6	-8.16
102	PC6	96	PC6	63	PC6	37	PC6	2152.6	71.92
103	PC7	97	PC7	64	PC7	38	PC7	2152.6	152
104	PC8	98	PC8	65	PC8	39	PC8	2152.6	357.52
105	PC9	99	PC9	66	PC9	40	PC9	2152.6	437.6
106	PA8	100	PA8	67	PA8	41	PA8	2152.6	517.68
107	DNU(1)							2152.6	599.98
108	PA9	101	PA9	68	PA9	42	PA9	2152.6	682.32
109	PA10	102	PA10	69	PA10	43	PA10	2152.6	762.4
110	PA11	103	PA11	70	PA11	44	PA11	2152.6	842.48
111	PA12	104	PA12	71	PA12	45	PA12	2152.6	1148.9
112	PA13	105	PA13	72	PA13	46	PA13	2152.6	1228.9
		106	NC	73	NC	-			
113	BYPASS(2)	-	V_{SS_2}		V_{SS_2}		V_{SS_2}	2152.6	1348.7
114	DNU(1)							2152.6	1556.6
115	V_{SS_2}	107	V_{SS_2}	74	V_{SS_2}	47	V_{SS_2}	2152.6	1764.8
116	V_{DD_2}	108	V_{DD_2}	75	V_{DD_2}	48	V_{DD_2}	2152.6	2002.3
117	PA14	109	PA14	76	PA14	49	PA14	2037.6	2117.3
118	DNU(1)							1955.3	2117.3

Table 5. Pad coordinates (continued)

Pad No.	Pad name	144 pins		100 pins		64 pins		Pad position	
		Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	X	Y
119	PA15	110	PA15	77	PA15	50	PA15	1873	2117.3
120	PC10	111	PC10	78	PC10	51	PC10	1513.4	2117.3
121	PC11	112	PC11	79	PC11	52	PC11	1433.4	2117.3
122	PC12	113	PC12	80	PC12	53	PC12	1353.3	2117.3
123	PD0	114	PD0	81	PD0	-		1273.2	2117.3
124	PD1	115	PD1	82	PD1	-		1193.1	2117.3
125	PD2	116	PD2	83	PD2	-		1113	2117.3
126	PD3	117	PD3	84	PD3	-		1033	2117.3
127	PD4	118	PD4	85	PD4	-		827.36	2117.3
128	PD5	119	PD5	86	PD5	-		747.36	2117.3
129	V_{SS_10}	120	V_{SS_10}	-		-		667.2	2117.3
130	V_{DD_10}	121	V_{DD_10}	-		-		561.92	2117.3
131	PD6	122	PD6	87	PD6	-		481.92	2117.3
132	PD7	123	PD7	88	PD7	-		401.84	2117.3
133	PG9	124	PG9	-		-		321.76	2117.3
134	PG10	125	PG10	-		-		241.68	2117.3
135	PG11	126	PG11	-		-		161.6	2117.3
136	PG12	127	PG12	-		-		81.52	2117.3
137	PG13	128	PG13	-		-		1.44	2117.3
138	PG14	129	PG14	-		-		-78.64	2117.3
139	V_{SS_11}	130	V_{SS_11}	-		-		-158.8	2117.3
140	V_{DD_11}	131	V_{DD_11}	-		-		-264.64	2117.3
141	PG15	132	PG15	-		-		-344.64	2117.3
142	PB3	133	PB3	89	PB3	55	PB3	-424.72	2117.3
143	PB4	134	PB4	90	PB4	56	PB4	-530	2117.3
144	PB5	135	PB5	91	PB5	57	PB5	-636.96	2117.3
145	PB6	136	PB6	92	PB6	58	PB6	-717.04	2117.3
146	PB7	137	PB7	93	PB7	59	PB7	-797.12	2117.3
147	BOOT0	138	BOOT0	94	BOOT0	60	BOOT0	-1128	2117.3
148	PB8	139	PB8	95	PB8	61	PB8	-1269.2	2117.3
149	PB9	140	PB9	96	PB9	62	PB9	-1349.3	2117.3
150	PE0	141	PE0	97	PE0	-		-1429.4	2117.3
151	PE1	142	PE1	98	PE1	-		-1509.4	2117.3

Table 5. Pad coordinates (continued)

Pad No.	Pad name	144 pins		100 pins		64 pins		Pad position	
		Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	X	Y
152	DNU[1]							-1591.9	2117.3
153	V_{SS_3}	143	V_{SS_3}	99	V_{SS_3}	63	V_{SS_3}	-1800.1	2117.3
154	V_{DD_3}	144	V_{DD_3}	100	V_{DD_3}	64	V_{DD_3}	-2037.6	2117.3

1. DNU stands for “do not use” (this pad should not be connected).
2. Bounded to V_{SS_2} in all packages.

4 Specific warning for die handling

4.1 Assembly qualification

Due to lower silicon rate in resin (percentage of silica in the mold compound) compared to plastic package, the COB (chip on board) assembly could be more sensitive to delamination.

Assembly reliability: as the assembly process is a key factor for module reliability, STMicroelectronics requires that the module is fully qualified, according to usual quality requirements.

For instance:

- thermal cycles: 2000 cycles, –40 °C/+150 °C
- temperature and humidity: 85°C, 85%RH
- construction analysis
- process and equipment FMEA's / control plan
- process flow / SPC capability

Running temperature extraction by resin must be checked as thermal resistance given for STMicroelectronics packages cannot be applied.

4.2 Traceability

ST requires a marking of the diffusion lot number and wafer number on the module for full traceability. This can be done directly on the PCB after assembly.

ST requires that the customer has his own traceability marking and a system with a full proof crosslink between the ST diffusion lot number and module number until delivery to the end customer.

4.3 Failure analysis

Failure analysis is done only if the reject rate reaches a 0.5% threshold.

Normally STMicroelectronics is not able to perform electrical retesting on dice, however electrical tests can be run if the customer fulfills the following requirements:

- End customer returns are first confirmed on the ST customer's manufacturing test equipment (ST requires a full application test coverage versus end customer application. ST declines responsibility for failures detected by end customers and not screened by ST customer production test).
- "Double pad implementation" is required (a specific layout on the application equivalent to the footprint of a standard JEDEC package taken from an equivalent package product). This allows the sawing of the application for failure analysis retesting in standard socketed equipment. For NVM failure analysis, a JTAG connection is a minimum requirement.

In addition, if the part is found good on ST's automatic test equipment (ATE), a method to replug the device into the module for further investigations is needed.

The customer must have the ability to remove the resin that covers the die (and keeps the application functional), making it possible to access all the die connections on the PCB side to allow probing if needed (contacts on PCB must be free of resin and varnish). This must be followed by visual inspection and continuity checking by the customer or assembly subcontractor.

Please contact your sales office for additional information, as before any failure analysis, STMicroelectronics will make a feasibility study for evaluation, which may lead to financial participation in some cases.

4.4 Flash memory recommendations

Retention guarantee is the same as for the assembled product. Special care must be taken due to sensitivity to UV exposure (refer to paragraph below).

Non-volatile memories (NVM) contain reference cells made of NVM cells and the system boot Flash, which are programmed during test at ST. If a die is exposed to UV light or X-rays with sufficient intensity and duration, these cells could be corrupted. This corruption can induce nonfunctionality of the entire memory just after the exposure or reduce the retention performance. In order to prevent corruption from occurring, special care must be taken to protect the die from long UV exposure.

For example:

- Assembly process can be critical, some plasma used for cleaning processes are known to generate UV light. Contact your plasma supplier for details
- PCB and glob top resin opacity to UV must be checked
- Extended storage in non-UV opaque packing

Normal neon light exposure during standard assembly process is sustainable without impact on retention.

4.5 Guarantee

With the above considerations, it is clear that the final guarantee of the microcontroller inside the application is shared between the customer and ST.

It is understood by customers that STMicroelectronics delivers parts screened at wafer level, therefore few rejects are expected to be found during the final screening after mounting.

STMicroelectronics will not endorse responsibility for those rejects below the maximum threshold of 0.5%.

5 Revision history

Table 6. Document revision history

Date	Revision	Changes
06-Oct-2008	1	Initial release.
27-Nov-2009	2	STM32F103ZET6DIE1 replaced by STM32F103EDIE. *Table 3: Ordering information* updated accordingly. Small text changes.

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