

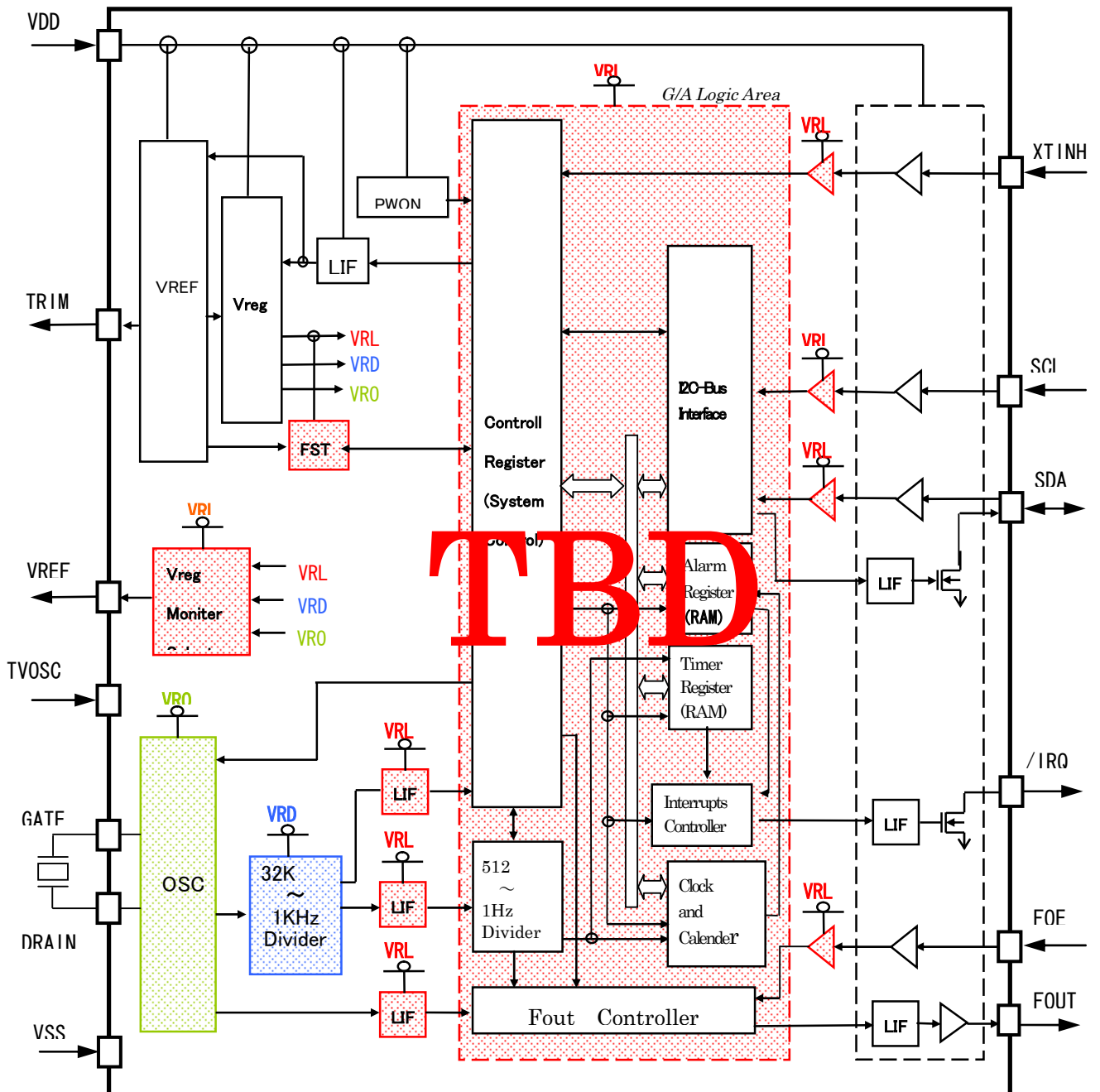
S1T542XXD0A00

Low-Current Consumption, Real-Time Clock IC (General-Purpose IC)

Preliminary

- Operating power voltage 1.6 to 5.5V (-40 to +85°C)
- Clock power voltage 1.2 to 5.5V (-40 to +85°C)
- Low-current consumption 0.25μA/Typ.
(During backup operation, VDD=3.0V, Ta=25°C)
(Depends on the characteristics of crystal oscillator used.)
- I2C Serial interface
- Output control 32.768kHz output function
- Real-time clock function
Clock and calendar function, automatic lead adjustment, alarm interrupt function, periodic timer interrupt and other functions
- Dropped power voltage detect function
- Shipment package Bear chips (solder bump)

■ System Block Diagram (Example)



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■ Pin Description

Pin Name	Pin No.	I/O	Description																						
Vss	1	Power supply	The ground (GND) pin. This is the 0V pin connected to the system GND. The IC substrate potential.																						
SDA	2	IN/OUT	The data I/O pin used for serial data transfer.																						
SCL	3	IN	The Shift Clock input pin used for serial data transfer. During writing, data is entered in the DIO pin at the rising edge of CLK signal. During reading, data is output at the DIO pin at the falling edge of CLK signal.																						
CE	4	IN	The Chip Enable pin. This pin has a built-in pull-down resistor. When the signal at CE pin is HIGH, this IC is access-enabled. When the CE pin is LOW, the DIO I/O pin is set to the high-impedance state and an input at the CLK input pin is inhibited.																						
FOE	5	IN	The input pin for output control at the FOUT output pin. In combination with FSEL1 and FSEL0 bits, the FOUT output can be selected as follows. <table border="1" data-bbox="552 815 1369 1061" style="margin: 10px auto;"> <thead> <tr> <th>FOE pin input</th> <th>FSEL1 bit</th> <th>FSEL0 bit</th> <th>FOUT pin Output</th> </tr> </thead> <tbody> <tr> <td rowspan="3">X (Don'tcare)</td> <td>0</td> <td>0</td> <td>32768Hz Output (C-MOS output)</td> </tr> <tr> <td>0</td> <td>1</td> <td>1024Hz Output (C-MOS output)</td> </tr> <tr> <td>1</td> <td>0</td> <td>1Hz Output (C-MOS output)</td> </tr> <tr> <td>HIGH</td> <td>1</td> <td>1</td> <td>32768Hz Output (C-MOS output) *1)</td> </tr> <tr> <td>LOW</td> <td>1</td> <td>1</td> <td>OFF (Hi-z)</td> </tr> </tbody> </table> <p>*1) If the FOE input pin is HIGH at the time of initial power-on (during power-on from 0V state), both FSEL1 and FSEL0 bits are set to 1 by the Power-On Reset function, and the 32.768 kHz output is selected.</p>	FOE pin input	FSEL1 bit	FSEL0 bit	FOUT pin Output	X (Don'tcare)	0	0	32768Hz Output (C-MOS output)	0	1	1024Hz Output (C-MOS output)	1	0	1Hz Output (C-MOS output)	HIGH	1	1	32768Hz Output (C-MOS output) *1)	LOW	1	1	OFF (Hi-z)
FOE pin input	FSEL1 bit	FSEL0 bit	FOUT pin Output																						
X (Don'tcare)	0	0	32768Hz Output (C-MOS output)																						
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	1	0	1Hz Output (C-MOS output)																						
HIGH	1	1	32768Hz Output (C-MOS output) *1)																						
LOW	1	1	OFF (Hi-z)																						
Vss	6	Power supply	The ground (GND) pin. This is the 0V pin connected to the system GND. The IC substrate potential.																						
/IRQ	7	OUT	Alarm, interval timer and other interrupt signals (LOW level) are output at this pin. This pin is the N-channel, open-drain output.																						
FOUT	8	OUT	The Clock Output pin having the Output Control function. The output is selected according to the FOE input pin state and FSEL1 and FSEL0 bit state. (For the frequency output selection and shutdown by combination of FOE input pin and FSEL1 and FSEL0 bit state, see the FOE Pin Description list.) This is the CMOS output IC.																						
XTINH	9	IN	The test signal input pin. Always connect to the Vss pin during normal operation.																						
VREF	10	OUT	The test signal output pin. This pin must always be open (disconnected) during normal operation.																						
VDD	11	Power supply	The power supply pin. Connect to the positive terminal of the power supply.																						
TVOSC	12	Power supply	The test pin. This pin must always be open (disconnected) during normal operation.																						
GATE	13	IN	The input pin of the crystal oscillator circuit.																						
DRAIN	14	OUT	The output pin of the crystal oscillator circuit.																						
TRIM	15	OUT	The test signal output pin. This pin must always be open (disconnected) during normal operation.																						

Note) Be sure to connect a 0.1μF or higher bypass capacitor to the position very close to the VDD to Vss circuit to stabilize the power supply.

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■ Recommended Operating Conditions

V_{SS}=0 V

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating power voltage	V _{ACC}	—	1.6	3.0	5.5	V
Clock power voltage	V _{CLK}	T _a = -40 to +85°C	1.2	3.0	5.5	V
Applied voltage during power-off	V _{PUP}	SDA, FOUT, /IRQ pins	—	—	5.5	V
Operating temperature range	T _{OPR}	Without condensing	-40	+25	+85	°C
Storage temperature	T _{STG}	—	-55	—	+125	°C

The “minimum” (Min) operating power voltage and the minimum clock power voltage mean the power voltages measured when their voltages are dropped from the operating state.

■ Frequency Characteristics

V_{SS}=0 V, crystal oscillator CI value = 40KΩ MAX.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillation frequency	f _o	—	32.768			kHz
Frequency voltage characteristics	f / V	T _a =+25 °C, V _{DD} = 2.0 V to 5.0 V	—	—	±2	× 10 ⁻⁶ / V
Frequency IC deviation	Δ f _o	T _a =+25 °C, V _{DD} = 3.0 V	-50	—	+50	× 10 ⁻⁶
Oscillation start time (1)	t _{STA1}	T _a =+25 °C, V _{DD} = 3.0 V	—	0.5	1.0	Sec
Oscillation start time (2)	t _{STA2}	T _a =-40 to +85°C, V _{DD} = 3.0 V	—	—	3.0	Sec
Built-in gate capacity	CG	Including pin capacity.	—	10	—	pF
Built-in drain capacity	CD	Including pin capacity.	—	7	—	pF

■ Power detection characteristics

V_{SS}=0 V, V_{DD}=1.6 to 5.5 V, T_a=-40 to +85°C unless otherwise notes.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Voltage drop detection	V _{LOW}	Between V _{DD} and V _{SS} pins	0.8	1.0	1.2	V

■ DC Characteristics 1

* V_{SS}=0 V, V_{DD}=1.6 to 5.5 V, T_a=-40 to +85°C unless otherwise notes.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Current consumption (1)	I _{DD1}	CE = OPEN (or V _{SS}) /IRQ = OFF FOUT ; Output OFF (Hi- z) Timer source clock = 1/60Hz	V _{DD} = 5 V	—	TBD	TBD	μA
Current consumption (2)	I _{DD2}		V _{DD} = 3 V	—	0.25	TBD	
Current consumption (3)	I _{DD3}	CE = OPEN (or V _{SS}) /IRQ = OFF, FOE = V _{DD} FOUT ; 32.768 kHz Output ON, CL = 0 pF	V _{DD} = 5 V	—	3.5	6.0	μA
Current consumption (4)	I _{DD4}		V _{DD} = 3 V	—	2.0	3.5	
Current consumption (5)	I _{DD5}	CE = OPEN (or V _{SS}) /IRQ = OFF, FOE = V _{DD} FOUT ; 32.768 kHz Output ON, CL = 30 pF	V _{DD} = 5 V	—	8.0	14.0	μA
Current consumption (6)	I _{DD6}		V _{DD} = 3 V	—	5.0	8.5	
Input leak current	I _{LK}	Input pins : V _{IN} =V _{DD} or V _{SS}	-0.5	—	0.5	μA	
Output leak current	I _{OZ}	Output pins, V _{OUT} = V _{DD} or V _{SS}	-0.5	—	0.5	μA	

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■ DC Characteristics 2

* VSS=0 V, VDD=1.6 to 5.5 V, Ta=-40 to +85°C unless otherwise notes.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
HIGH input voltage	VIH1	Input pin	$0.70 \times V_{DD}$	—	$V_{DD} + 0.3$	V	
	VIH2	Input pin (5 V ± 10 %)	$0.75 \times V_{DD}$	—	$V_{DD} + 0.3$	V	
LOW input voltage	VIL1	Input pin	$V_{SS} - 0.3$	—	$0.30 \times V_{DD}$	V	
	VIL2	Input pin (5 V ± 10 %)	$V_{SS} - 0.3$	—	$0.25 \times V_{DD}$	V	
HIGH output voltage	VOH1	FOUT pins	VDD = 5 V, IOH = -1 mA	4.5	—	5.0	V
	VOH2		VDD = 3 V, IOH = -1 mA	2.2	—	3.0	
	VOH3		VDD = 3 V, IOH = -100 μA	2.9	—	3.0	
LOW output voltage	VOL1	FOUT pins	VDD = 5 V, IOL = 1 mA	VSS	—	VSS+0.5	V
	VOL2		VDD = 3 V, IOL = 1 mA	VSS	—	VSS+0.8	
	VOL3		VDD = 3 V, IOL = 100 μA	VSS	—	VSS+0.1	
	VOL4	SDA, /IRQ pins	VDD = 5 V, IOL = 1 mA	VSS	—	VSS+0.25	
	VOL5		VDD = 3 V, IOL = 1 mA	VSS	—	VSS+0.4	
	VOL6	SDA pins	VDD ≥ 2 V, IOL = 3 mA	VSS	—	VSS+0.4	
Input resistance (1)	RDWN1	CE pins	VDD = 5 V	75	150	300	kΩ
Input resistance (2)	RDWN2	VIN = VDD	VDD = 3 V	150	300	600	
Input capacity	CI	SCL,CE,FOE pins	Freq. = 1 MHz	—	—	15	pF
Output capacity	CO	/IRQ,SDA,FOUT pins	Ta = 25 °C	—	—	15	

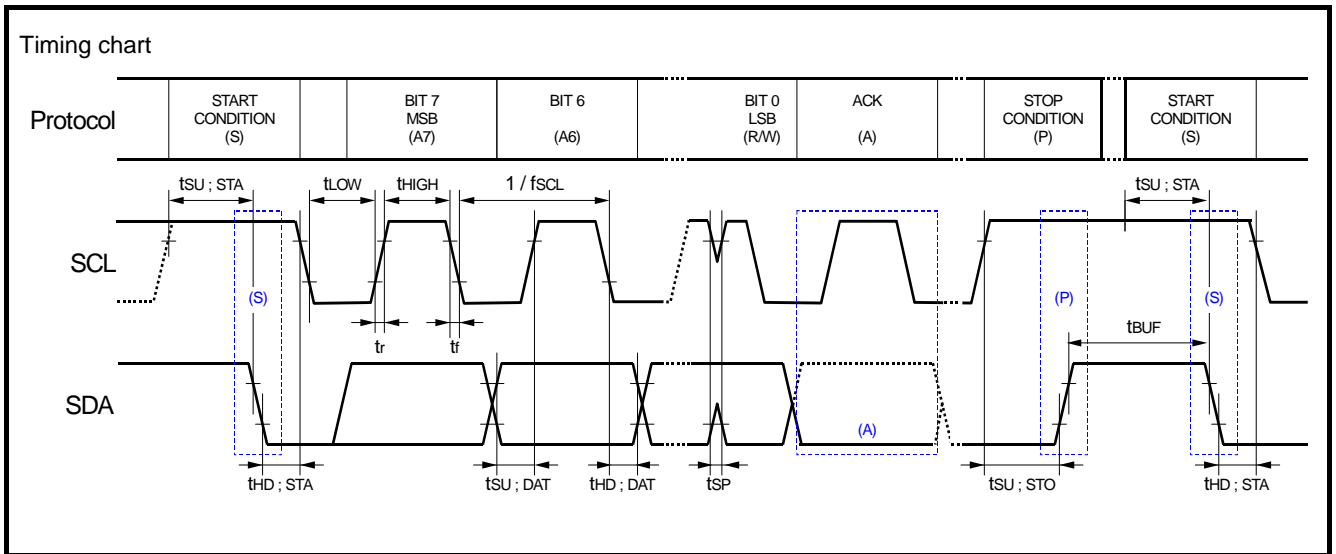
■ AC Characteristics

VSS=0V, VDD=1.6V~5.5V, Ta=-40 to +85°C unless otherwise noted.

Item	Symbol	100 kHz access (Standard-Mode)		400 kHz access (Fast-Mode)		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	fSCL		100		400	kHz
Start condition setup time	tSU:STA	4.7		0.6		μs
Start condition hold time	tHD:STA	4.0		0.6		μs
Data setup time	tSU:DAT	250		100		ns
Data hold time	tHD:DAT	0		0		ns
Halt condition setup time	tSU:STO	4.0		0.6		μs
Bus free time between start condition and halt condition	tBUF	4.7		1.3		μs
SCL " L " time	tLOW	4.7		1.3		μs
SCL " H " time	tHIGH	4.0		0.6		μs
SCL, SDA Start-up time	tr		1.0		0.3	μs
SCL, SDA Standing lowering time	tf		0.3		0.3	μs
Permission spike time on bus	tSP		50		50	ns

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
FOUT Duty	Duty	50% VDD level	40	50	60	%

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Attention: Please end the access to this device within one second from sending of start condition to the sending of the STOP condition after access complete. In the case of over 1 second, I2C bus interface of RTC is reset by the surveillance timer of the inside.

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