S1T542XXD0A00

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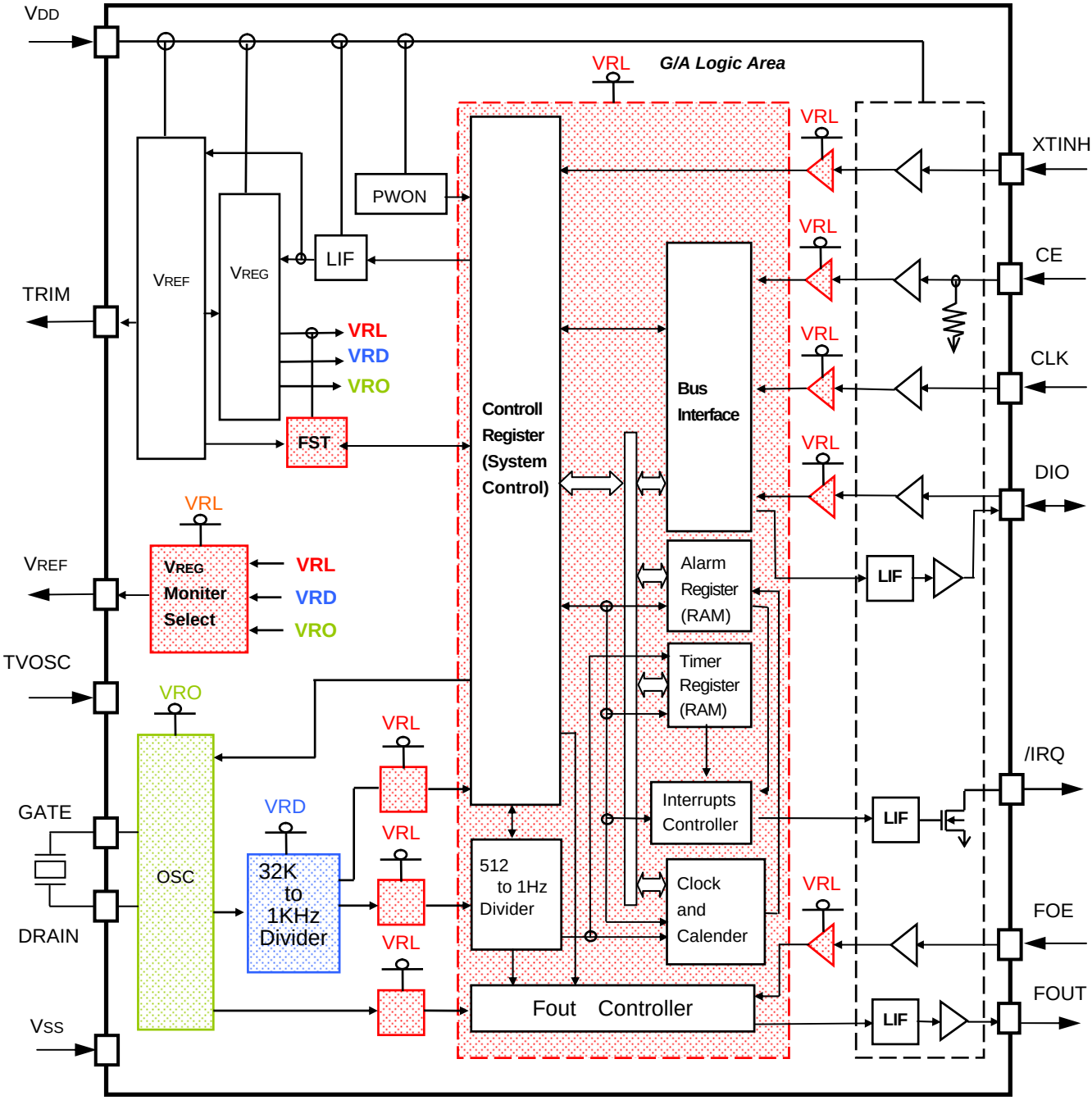
Low-Current Consumption, Real-Time Clock IC (General-Purpose IC)

Preliminary

- Operating power voltage 1.6 to 5.5V (-40 to +85°C)
- Clock power voltage 1.2 to 5.5V (-40 to +85°C)
- Low-current consumption 0.20μA/Typ.
  (During backup operation, V_{DD}=3.0V, T_a=25°C)
  (Depends on the characteristics of crystal oscillator used.)
- 3-wire Serial interface
- Output control 32.768kHz output function
- Real-time clock function
  Clock and calendar function, automatic lead adjustment, alarm interrupt function, periodic timer interrupt and other functions
- Dropped power voltage detect function
- Shipment package Bear chips (solder bump)

■ System Block Diagram (Example)



■ Pin Description

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>I/O</th><th>Description</th></tr>
<tr><td>VSS</td><td>1</td><td>Power supply</td><td>The ground (GND) pin. This is the 0V pin connected to the system GND. The IC substrate potential.</td></tr>
<tr><td>DIO</td><td>2</td><td>IN/OUT</td><td>The data I/O pin used for serial data transfer.</td></tr>
<tr><td>CLK</td><td>3</td><td>IN</td><td>The Shift Clock input pin used for serial data transfer.
During writing, data is entered in the DIO pin at the rising edge of CLK signal. During reading, data is output at the DIO pin at the falling edge of CLK signal.</td></tr>
<tr><td>CE</td><td>4</td><td>IN</td><td>The Chip Enable pin. This pin has a built-in pull-down resistor.
When the signal at CE pin is HIGH, this IC is access-enabled.
When the CE pin is LOW, the DIO I/O pin is set to the high-impedance state and an input at the CLK input pin is inhibited.</td></tr>
<tr><td>FOE</td><td>5</td><td>IN</td><td>The input pin for output control at the FOUT output pin.
In combination with FSEL1 and FSEL0 bits, the FOUT output can be selected as follows.
<table>
<tr><th>FOE pin input</th><th>FSEL1 bit</th><th>FSEL0 bit</th><th>FOUT pin Output</th></tr>
<tr><td rowspan="3">X (Don’tcare)</td><td>0</td><td>0</td><td>32768Hz Output (C-MOS output)</td></tr>
<tr><td>0</td><td>1</td><td>1024Hz Output (C-MOS output)</td></tr>
<tr><td>1</td><td>0</td><td>1Hz Output (C-MOS output)</td></tr>
<tr><td>HIGH</td><td>1</td><td>1</td><td>32768Hz Output (C-MOS output) *1）</td></tr>
<tr><td>LOW</td><td>1</td><td>1</td><td>OFF (Hi-z)</td></tr>
</table>
*1) If the FOE input pin is HIGH at the time of initial power-on (during power-on from 0V state), both FSEL1 and FSEL0 bits are set to 1 by the Power-On Reset function, and the 32.768 kHz output is selected.</td></tr>
<tr><td>VSS</td><td>6</td><td>Power supply</td><td>The ground (GND) pin. This is the 0V pin connected to the system GND. The IC substrate potential.</td></tr>
<tr><td>/IRQ</td><td>7</td><td>OUT</td><td>Alarm, interval timer and other interrupt signals (LOW level) are output at this pin.
This pin is the N-channel, open-drain output.</td></tr>
<tr><td>FOUT</td><td>8</td><td>OUT</td><td>The Clock Output pin having the Output Control function.
The output is selected according to the FOE input pin state and FSEL1 and FSEL0 bit state.
(For the frequency output selection and shutdown by combination of FOE input pin and FSEL1 and FSEL0 bit state, see the FOE Pin Description list.)
This is the CMOS output IC.</td></tr>
<tr><td>XTINH</td><td>9</td><td>IN</td><td>The test signal input pin. Always connect to the VSS pin during normal operation.</td></tr>
<tr><td>VREF</td><td>10</td><td>OUT</td><td>The test signal output pin. This pin must always be open (disconnected) during normal operation.</td></tr>
<tr><td>VDD</td><td>11</td><td>Power supply</td><td>The power supply pin. Connect to the positive terminal of the power supply.</td></tr>
<tr><td>TVOSC</td><td>12</td><td>Power supply</td><td>The test pin. This pin must always be open (disconnected) during normal operation.</td></tr>
<tr><td>GATE</td><td>13</td><td>IN</td><td>The input pin of the crystal oscillator circuit.</td></tr>
<tr><td>DRAIN</td><td>14</td><td>OUT</td><td>The output pin of the crystal oscillator circuit.</td></tr>
<tr><td>TRIM</td><td>15</td><td>OUT</td><td>The test signal output pin. This pin must always be open (disconnected) during normal operation.</td></tr>
</table>

Note) Be sure to connect a 0.1μF or higher bypass capacitor to the position very close to the VDD to VSS circuit to stabilize the power supply.

■ Recommended Operating Conditions

V_{SS}=0 V

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating power voltage	V_{ACC}	—	1.6	3.0	5.5	V
Clock power voltage	V_{CLK}	T_a = -40 to +85°C	1.2	3.0	5.5	V
Applied voltage during power-off	V_{PUP}	FOUT, /IRQ pins	—	—	5.5	V
Operating temperature range	T_{OPR}	Without condensing	–40	+25	+85	°C
Storage temperature	T_{STG}	—	–55	—	+125	°C

The “minimum” (Min) operating power voltage and the minimum clock power voltage mean the power voltages measured when their voltages are dropped from the operating state.

■ Frequency Characteristics

V_{SS}=0 V, crystal oscillator CI value = 40 kΩ Max.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillation frequency	fo	—		32.768		kHz
Frequency voltage characteristics	f / V	T_a=+25 °C,V_{DD} = 2.0 V to 5.0 V	—	—	±2	× 10^{-6} / V
Frequency IC deviation	Δ fo	T_a=+25 °C,V_{DD} = 3.0 V	-50	—	+50	× 10^{-6}
Oscillation start time (1)	t_{STA1}	T_a=+25 °C,V_{DD} = 3.0 V	—	0.5	1.0	Sec
Oscillation start time (2)	t_{STA2}	T_a=-40 to +85°C , V_{DD} = 3.0 V	—	—	3.0	Sec
Built-in gate capacity	CG	Including pin capacity.	—	10	—	pF
Built-in drain capacity	CD	Including pin capacity.	—	7	—	pF

■ Power detection characteristics

V_{SS}=0 V, V_{DD}=1.6 to 5.5 V, T_a=-40 to +85°C unless otherwise notes.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Voltage drop detection	V_{LOW}	Between V_{DD} and V_{SS} pins	0.8	1.0	1.2	V

■ DC Characteristics 1

* V_{SS}=0 V, V_{DD}=1.6 to 5.5 V, T_a=-40 to +85°C unless otherwise notes.

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Current consumption (1)	I_{DD1}	CE = OPEN (or V_{SS}) /IRQ = OFF FOUT ; Output OFF (Hi- z) Timer source clock = 1/60Hz	V_{DD} = 5 V	—	TBD	TBD	µA
Current consumption (2)	I_{DD2}		V_{DD} = 3 V	—	0.20	TBD	
Current consumption (3)	I_{DD3}	CE = OPEN (or V_{SS}) /IRQ = OFF, FOE = V_{DD} FOUT ; 32.768 kHz Output ON , CL = 0 pF	V_{DD} = 5 V	—	3.5	6.0	µA
Current consumption (4)	I_{DD4}		V_{DD} = 3 V	—	2.0	3.5	
Current consumption (5)	I_{DD5}	CE = OPEN (or V_{SS}) /IRQ = OFF, FOE = V_{DD} FOUT ; 32.768 kHz Output ON , CL = 30 pF	V_{DD} = 5 V	—	8.0	14.0	µA
Current consumption (6)	I_{DD6}		V_{DD} = 3 V	—	5.0	8.5	
Input leak current	I_{LK}	Input pins except for CE: V_{IN}=V_{DD} or V_{SS}		-0.5	—	0.5	µA
Output leak current	I_{OZ}	Output pins, V_{OUT} = V_{DD} or V_{SS}		-0.5	—	0.5	µA

■ DC Characteristics 2

* V_{SS}=0 V, V_{DD}=1.6 to 5.5 V, T_a=-40 to +85°C unless otherwise notes.

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH input voltage	V_{IH1}	Input pin		0.70 × V_{DD}	—	V_{DD} + 0.3	V
	V_{IH2}	Input pin (5 V ± 10 %)		0.75 × V_{DD}	—	V_{DD} + 0.3	V
LOW input voltage	V_{IL1}	Input pin		V_{SS} - 0.3	—	0.30 × V_{DD}	V
	V_{IL2}	Input pin (5 V ± 10 %)		V_{SS} - 0.3	—	0.25 × V_{DD}	V
HIGH output voltage	V_{OH1}	DIO, FOUT pins	V_{DD} = 5 V, I_{OH} = -1 mA	4.5	—	5.0	V
	V_{OH2}		V_{DD} = 3 V, I_{OH} = -1 mA	2.2	—	3.0	
	V_{OH3}		V_{DD} = 3 V, I_{OH} = -100 μA	2.9	—	3.0	
LOW output voltage	V_{OL1}	DIO, FOUT pins	V_{DD} = 5 V, I_{OL} = 1 mA	V_{SS}	—	V_{SS}+0.5	V
	V_{OL2}		V_{DD} = 3 V, I_{OL} = 1 mA	V_{SS}	—	V_{SS}+0.8	
	V_{OL3}		V_{DD} = 3 V, I_{OL} = 100 μA	V_{SS}	—	V_{SS}+0.1	
	V_{OL4}	/IRQ pins	V_{DD} = 5 V, I_{OL} = 1 mA	V_{SS}	—	V_{SS}+0.25	
	V_{OL5}		V_{DD} = 3 V, I_{OL} = 1 mA	V_{SS}	—	V_{SS}+0.4	
Input resistance (1)	RDWN1	CE pins V_{IN} = V_{DD}	V_{DD} = 5 V	75	150	300	kΩ
Input resistance (2)	RDWN2		V_{DD} = 3 V	150	300	600	
Input capacity	CI	CLK,CE,FOE pins	Freq. = 1 MHz	—	—	15	pF
Output capacity	CO	/IRQ,DIO,FOUT pins	T_a = 25 °C	—	—	15	

■ AC Characteristics

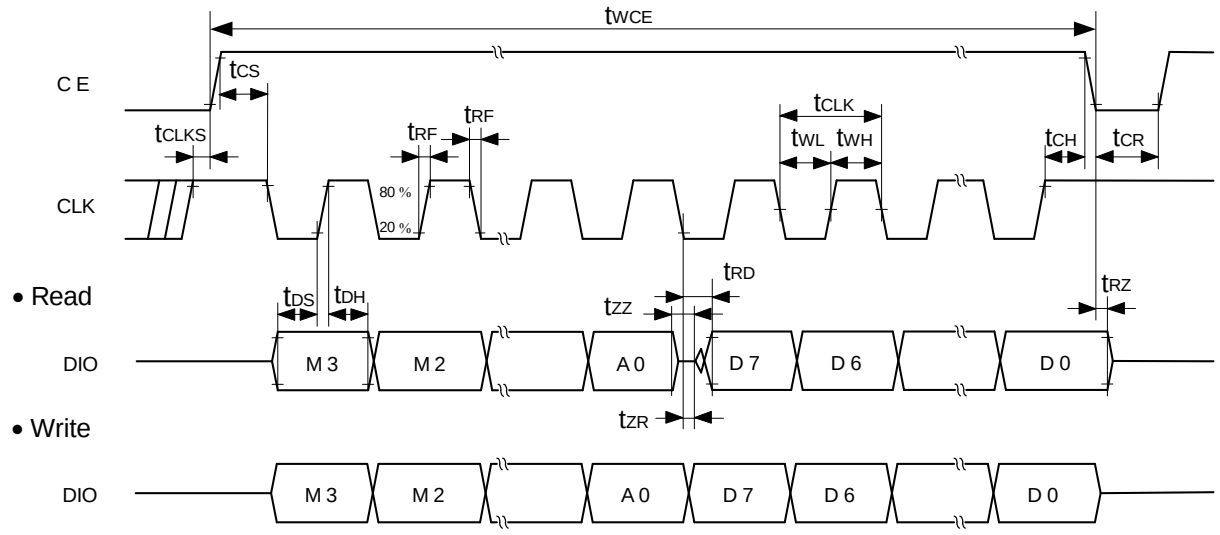
* V_{SS}=0V, T_a=-40 to +85°C unless otherwise noted.

Item	Symbol	Conditions	V_{DD}=1.8V ± 0.2V		V_{DD}=3.0V ±10%		V_{DD}=5.0V ±10%		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
CLK clock frequency	t_{CLK}	—	1000	—	500	—	350	—	ns
CLK High pulse width	t_{WH}	—	450	—	220	—	155	—	ns
CLK Low pulse width	t_{WL}	—	450	—	220	—	155	—	ns
CLK setup time	t_{CLKS}	—	100	—	50	—	25	—	ns
CE setup time	t_{CS}	—	400	—	200	—	150	—	ns
CE hold time	t_{CH}	—	400	—	200	—	100	—	ns
CE recovery time	t_{CR}	—	600	—	300	—	200	—	ns
CE recovery time	t_{WCE}	—	—	0.95	—	0.95	—	0.95	s
Write data setup time	t_{DS}	—	200	—	100	—	50	—	ns
Write data hold time	t_{DH}	—	200	—	100	—	50	—	ns
Read data delay time	t_{RD}	CL=50 pF	—	400	—	200	—	150	ns
DO output switching time	t_{ZR}	—	5	100	5	50	5	25	ns
DO output disable time	t_{RZ}	CL=50 pF RL=10 kΩ	—	400	—	200	—	100	ns
DI/DO conflict-avoiding time	t_{ZZ}	—	0	—	0	—	0	—	ns

* Use the V_{DD}=1.8±0.2V standard for V_{DD}=2.0 to 2.7V, and use the V_{DD}=3V±10% standard for V_{DD}=3.3 to 4.5V.
* Set the input signal rising/falling time (t_{RF}) to 15 nsec or less.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
FOUT duty ratio	Duty	50% VDD Level	40	50	60	%

Timing Chart



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