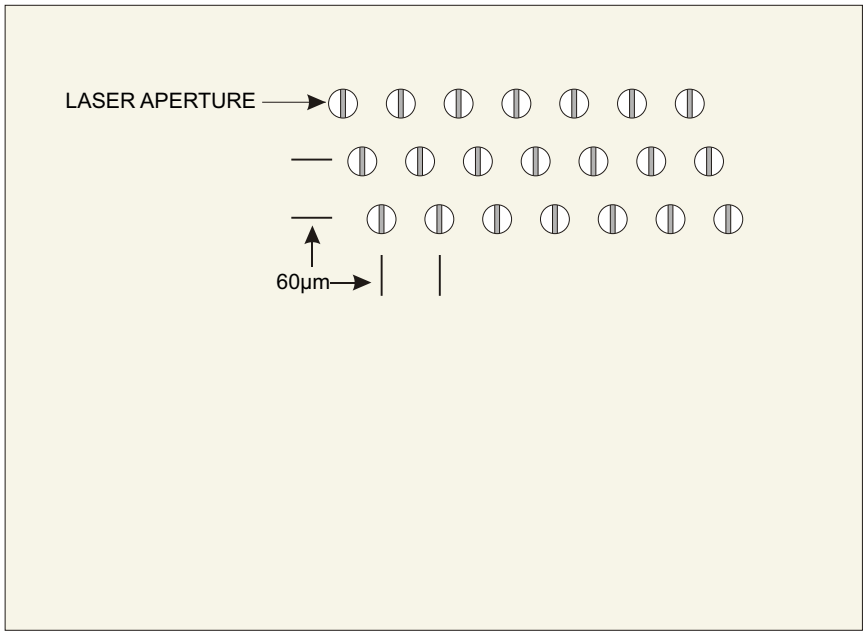
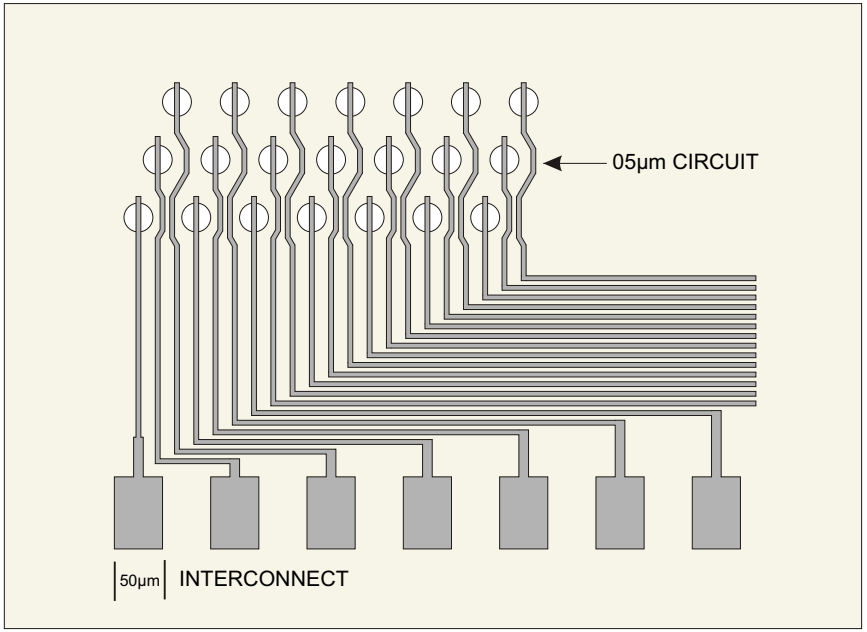
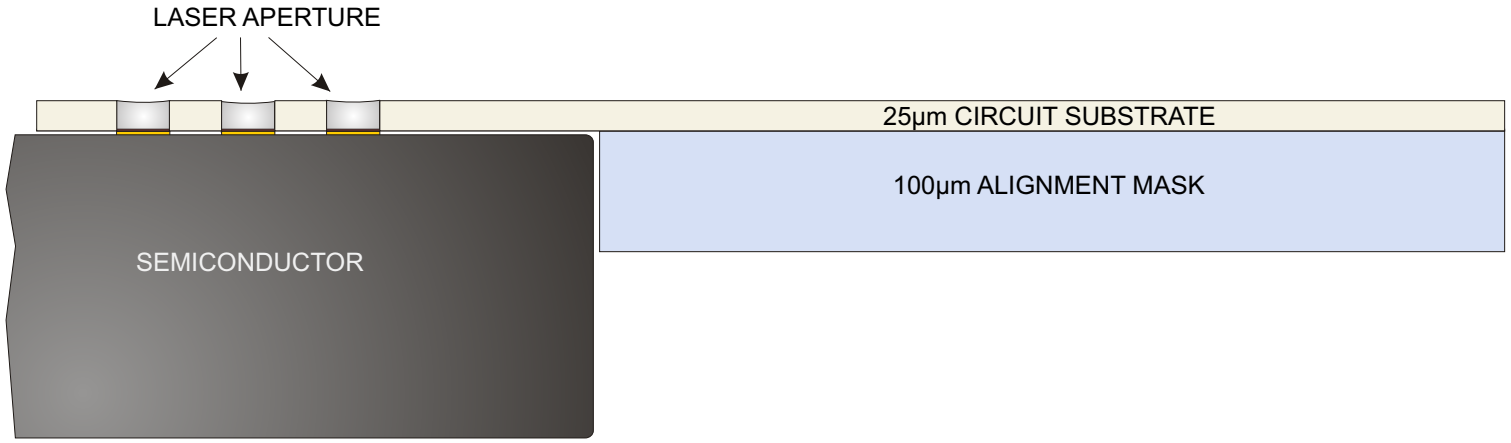
60 MICRON INTERCONNECT FOR 3 TIER SEMICONDUCTOR



TOP

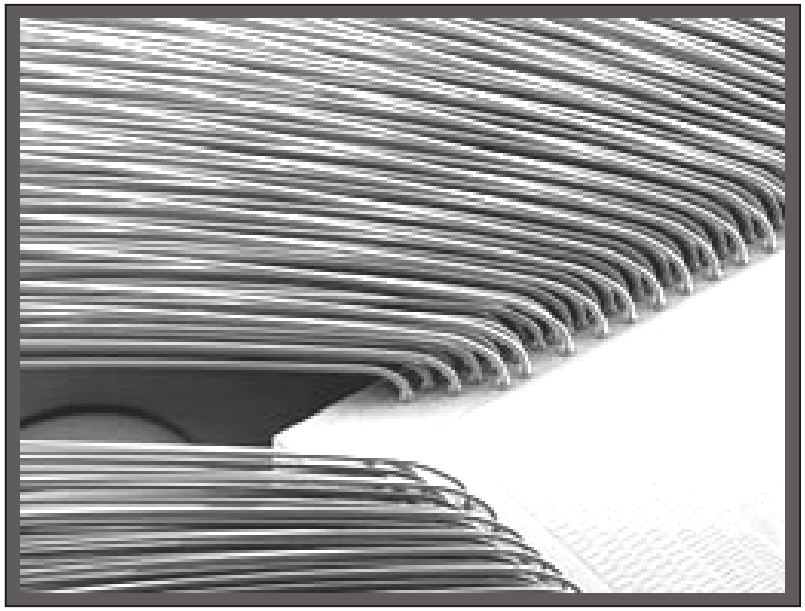


BOTTOM



K&S WIRE BOND DEVICE

Current multi-tier devices in production consist of triple-tier bond-pad layouts (Fig. 1), and quad-tier die are on the horizon. Chipmakers are finding that the multi-tier layout is more feasible from a wire-bonding standpoint than continuing to reduce pad pitches, since a triple tier of 60 µm pitched bond pads can have an effective 20 µm pitch. The additional silicon required to accommodate more bond pads is a worthwhile trade-off for robustness in the wire-bonding process. Another advantage of the multi-tier package is that conventional materials, with respect to capillaries and wire, can be used to assemble these packages. The fragility of ultrafine -pitch capillaries and wire is not well suited for production.



The emergence of multi-tier packages has also created new challenges in wire-loop shaping.[1] The use of multiple layers of wires in a single device is difficult because the loop shapes must have sufficient clearance to avoid wire shorting while limiting the overall height of the package. To achieve these goals, the lower layers of wires must be kept as low as possible and the upper layers of wires must employ higher loop heights and maintain longer flat lengths to traverse the lower layers.